Electronics II – Chapter 9

Counters

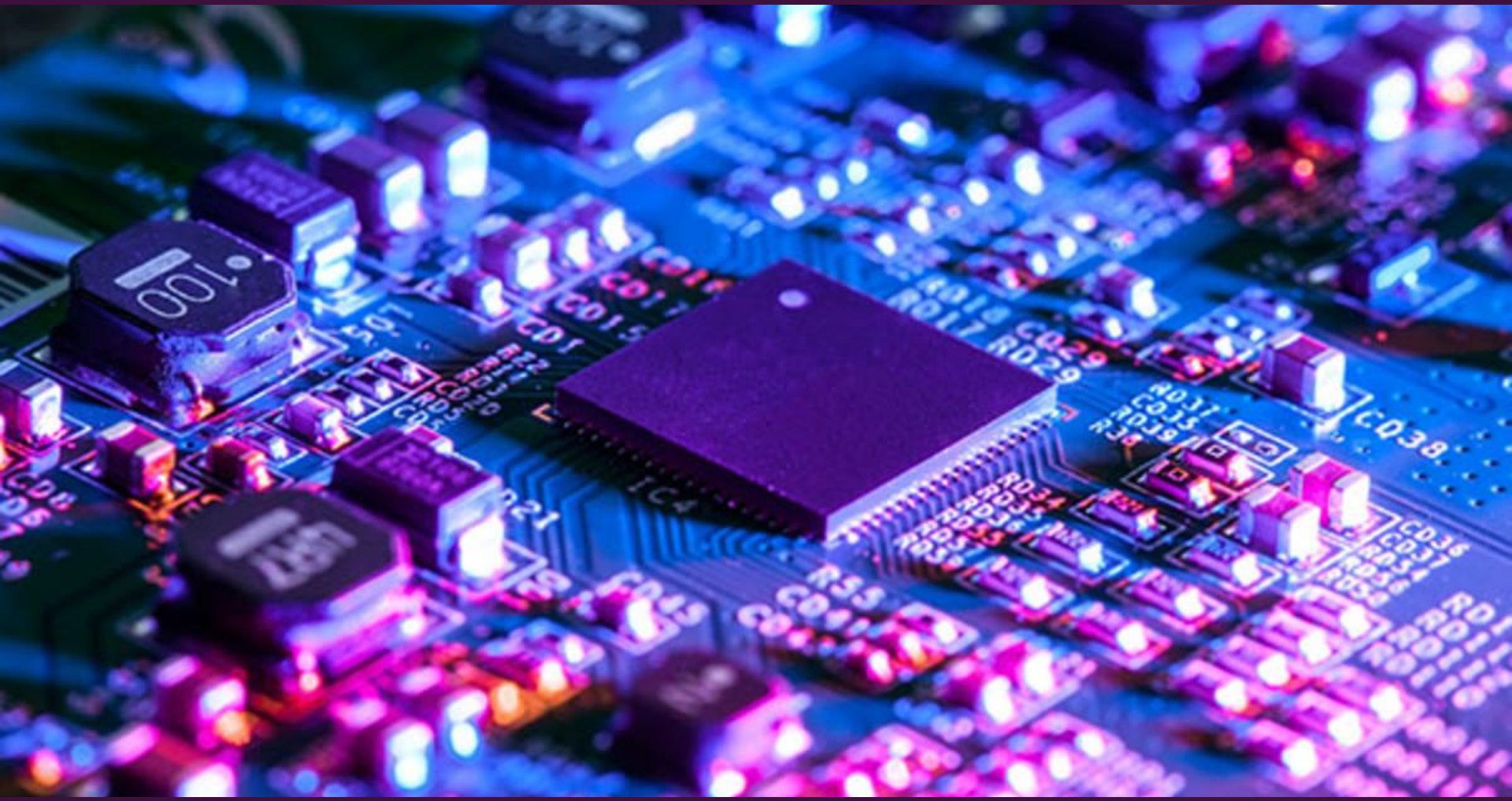
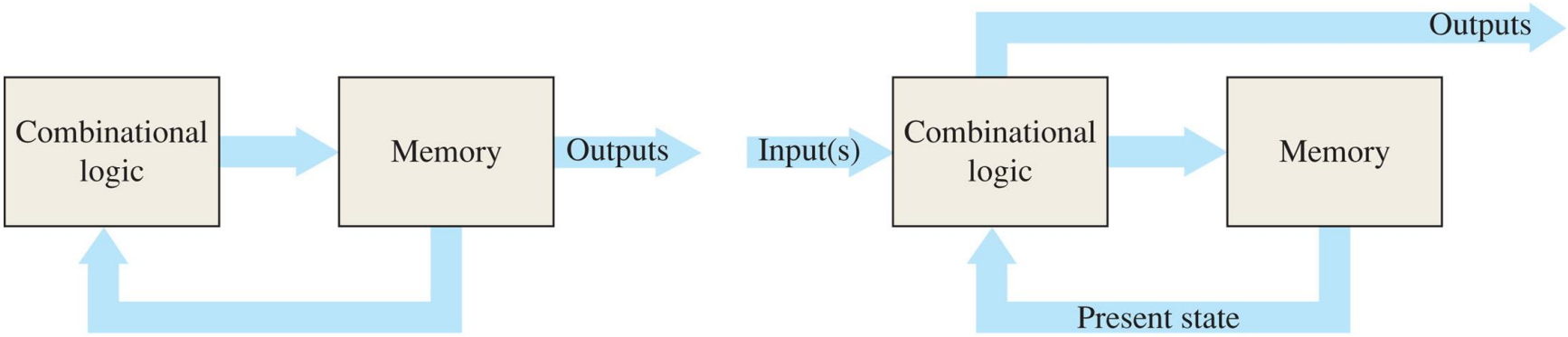


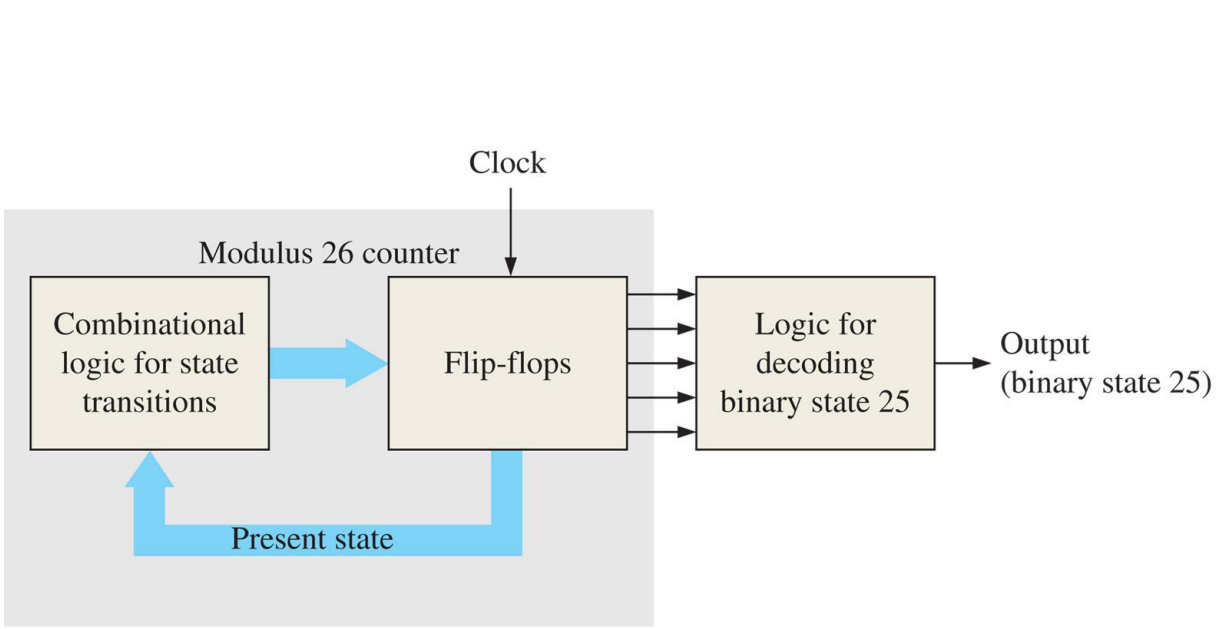
FIGURE 9-1 Two types of sequential logic.



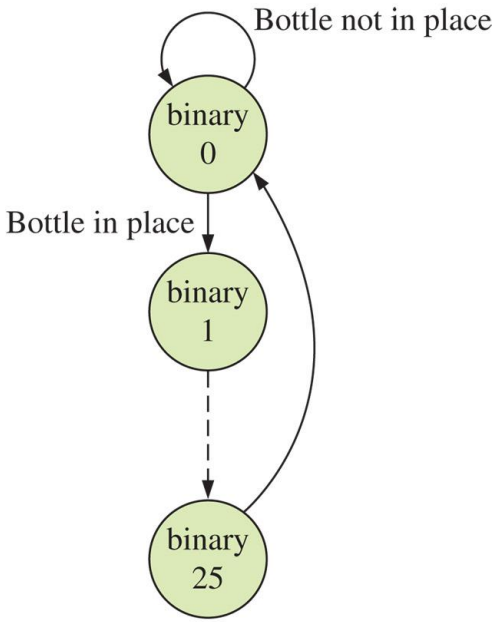
(a) Moore machine

(b) Mealy machine

FIGURE 9-2 A fixed-modulus binary counter as an example of a Moore state machine. The dashed line in the state diagram means the states between binary 1 and 25 are not shown for simplicity.

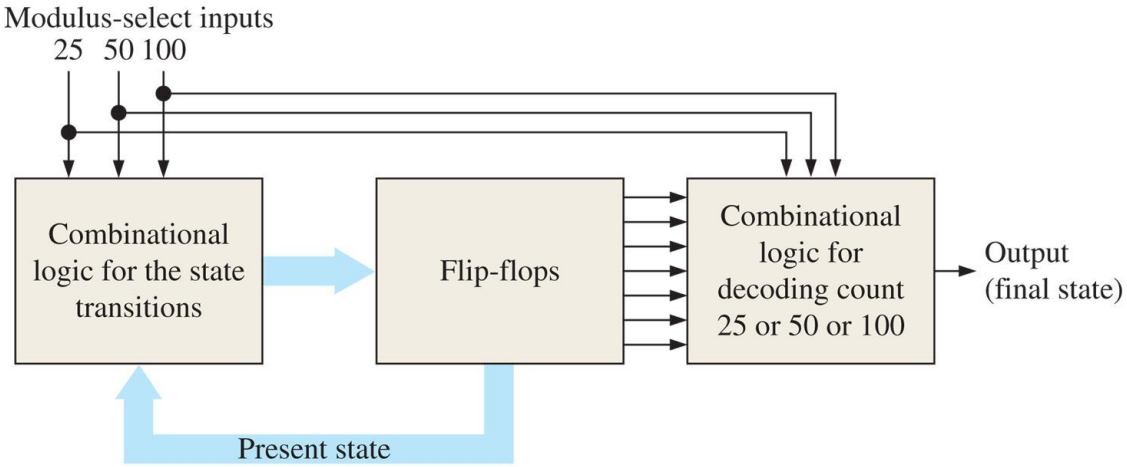


(a) Moore machine

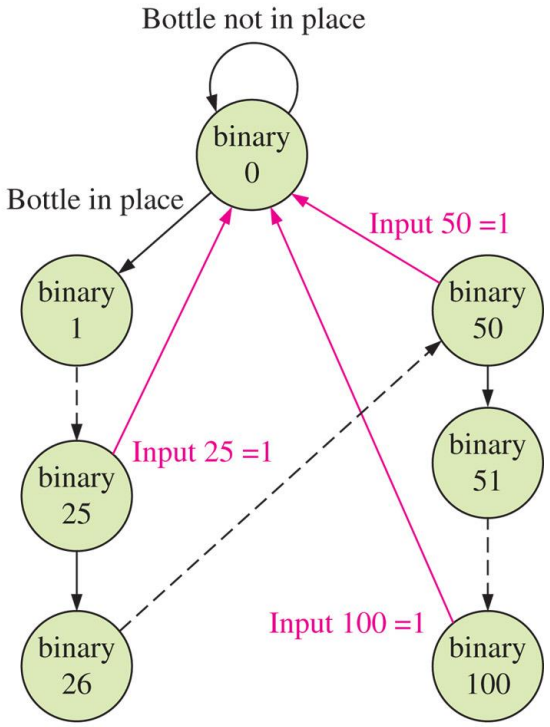


(b) State diagram

FIGURE 9-3 A variable-modulus binary counter as an example of a Mealy state machine. The red arrows in the state diagram represent the recycle paths that depend on the input number. The black dashed lines mean the interim states are not shown for simplicity.



(a) Mealy machine



(b) State diagram

FIGURE 9-4 A 2-bit asynchronous binary counter.

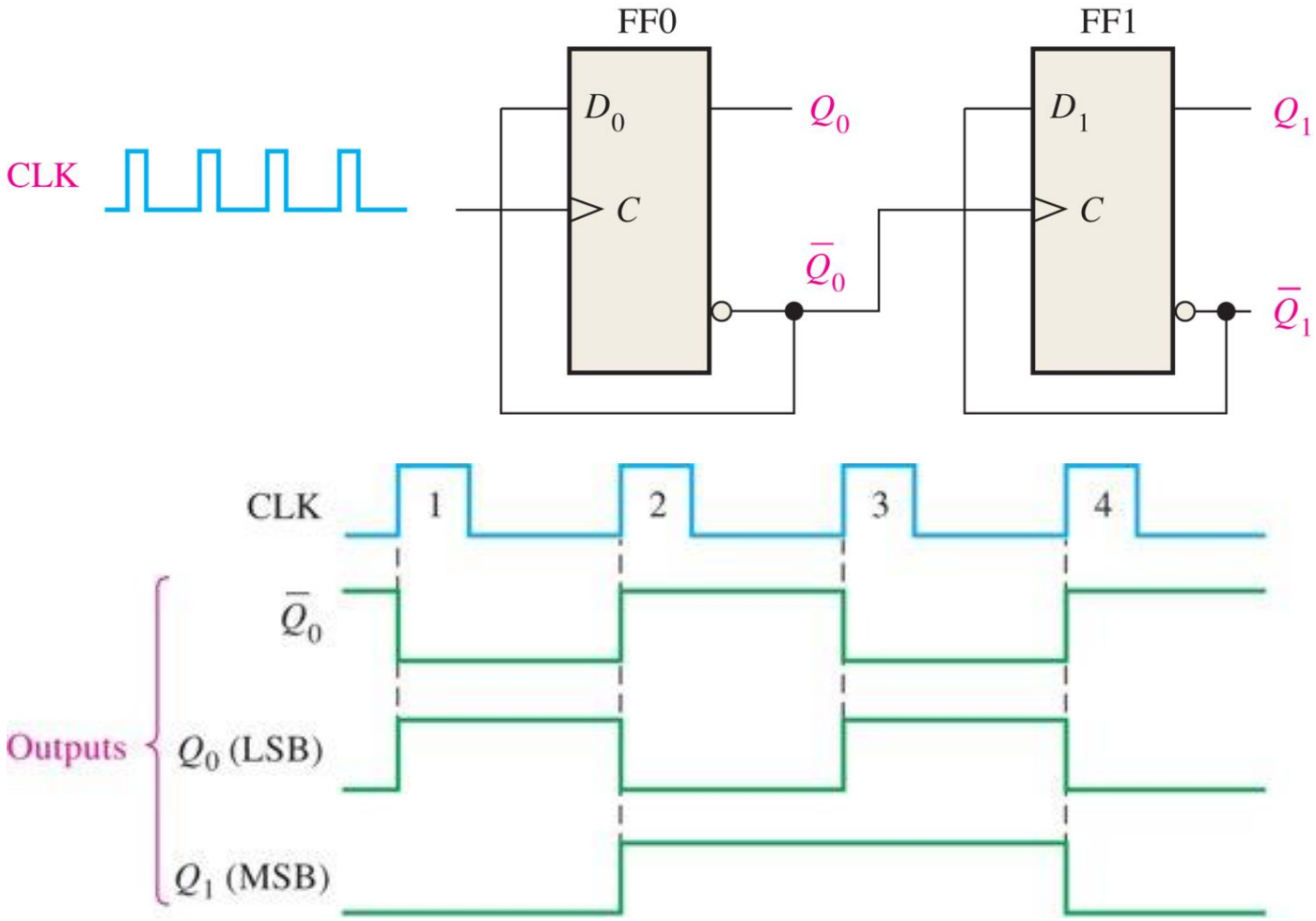


FIGURE 9-6 Three-bit asynchronous binary counter and its timing diagram for one cycle.

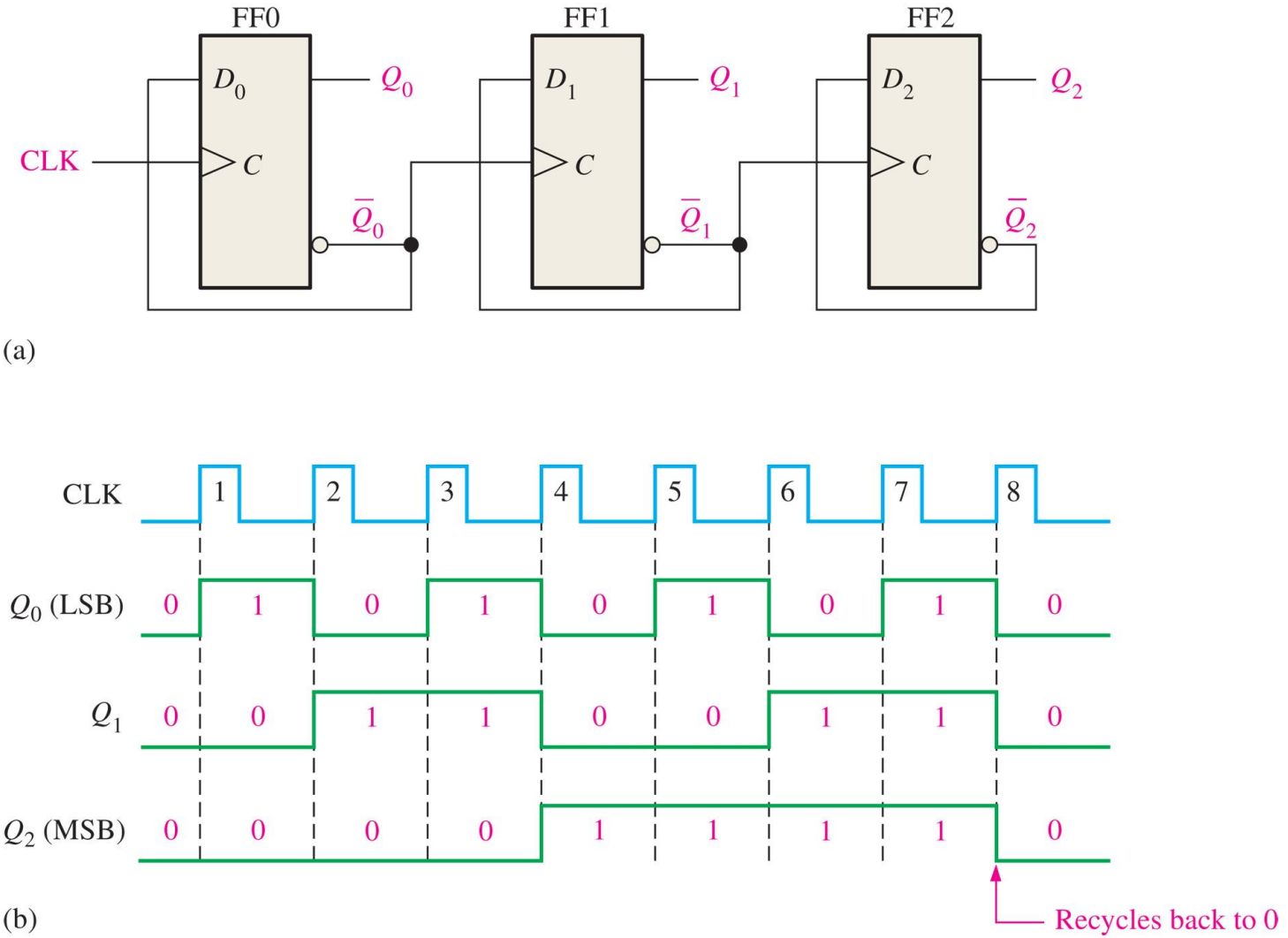


FIGURE 9-7 Propagation delays in a 3-bit asynchronous (ripple-clocked) binary counter.

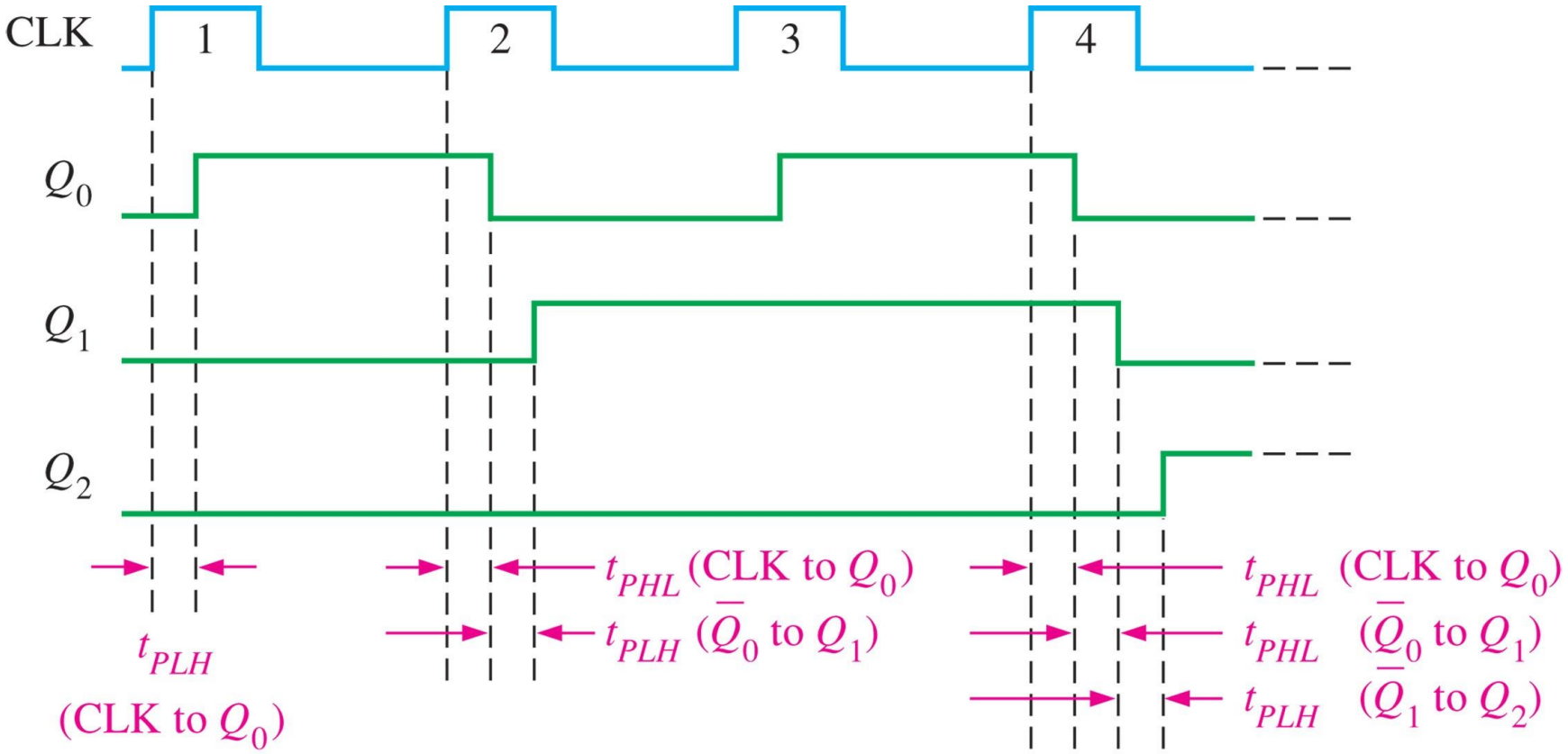


FIGURE 9-8 Four-bit asynchronous binary counter and its timing diagram.

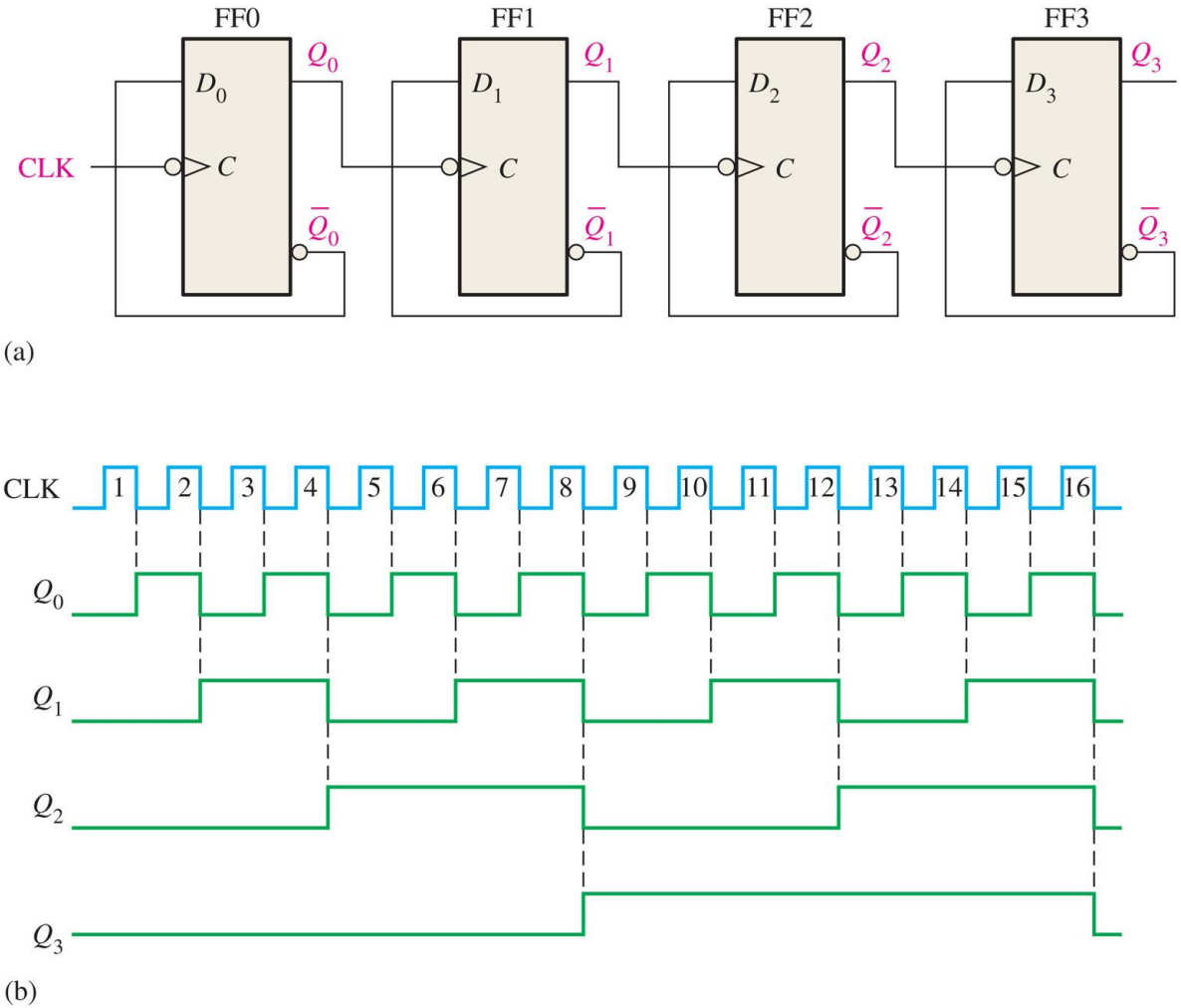


FIGURE 9-9 An asynchronously clocked decade counter with asynchronous recycling.

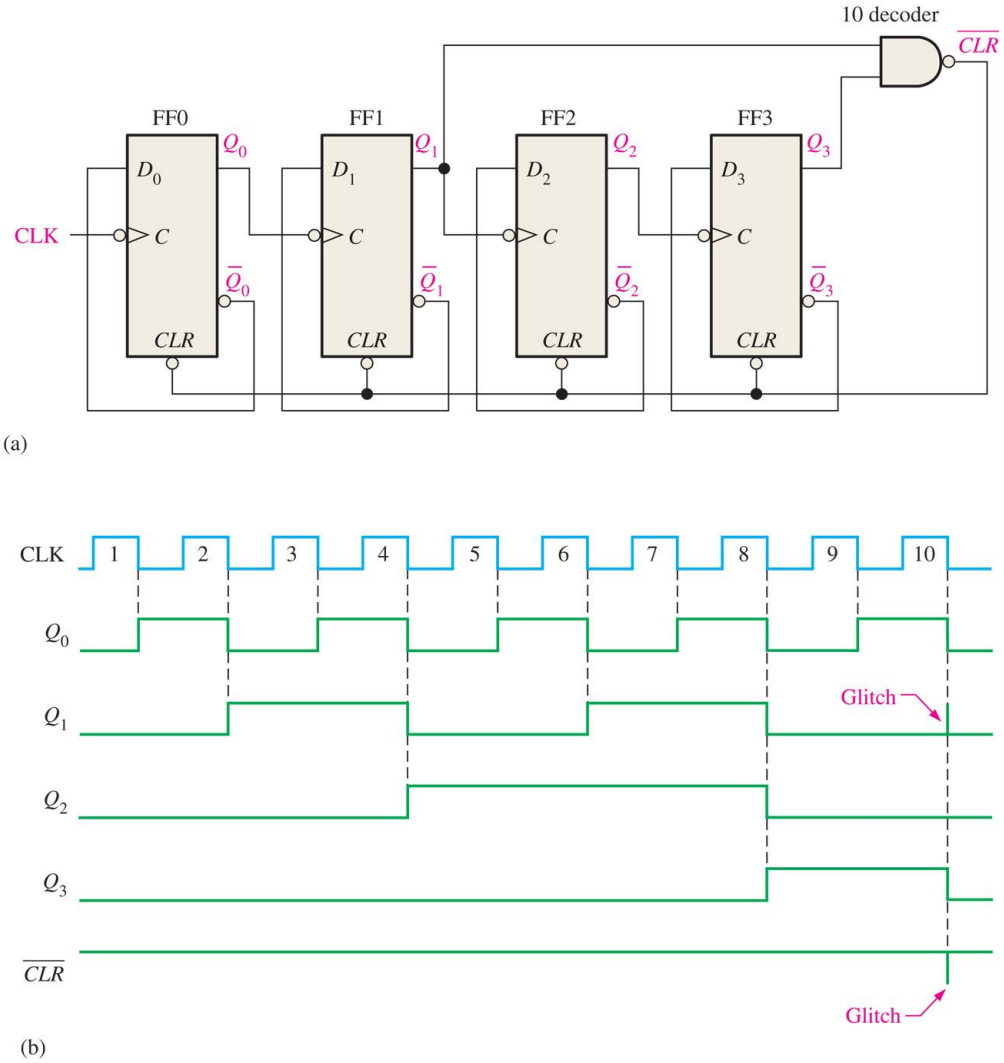
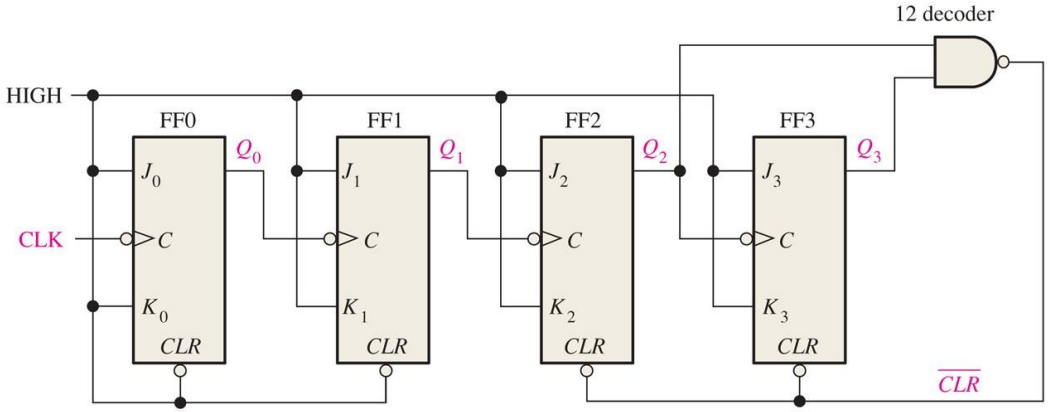
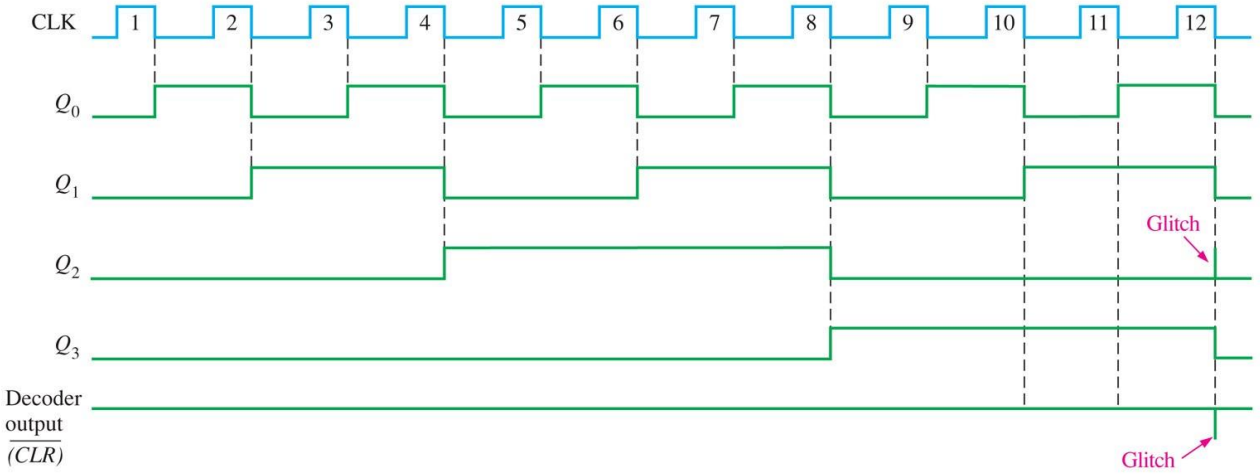


FIGURE 9-10 Asynchronously clocked modulus-12 counter with asynchronous recycling.

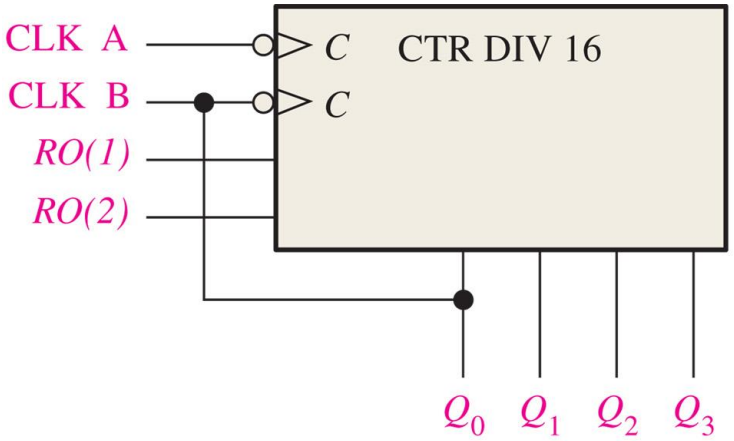


(a)

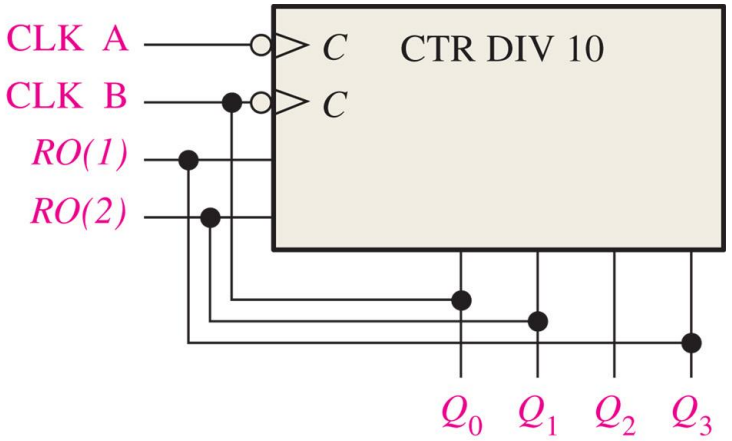


(b)

FIGURE 9-11 Two configurations of the 74HC93 asynchronous counter. (The qualifying label, CTR DIV *n*, indicates a counter with *n* states.)

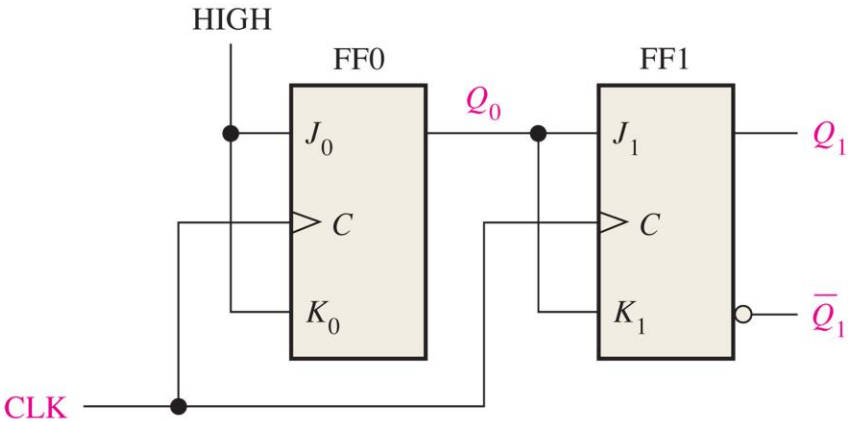


(a) 74HC93 connected as a modulus-16 counter

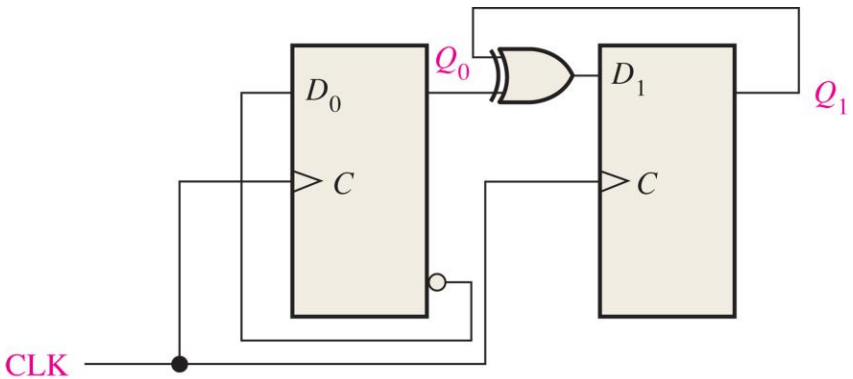


(b) 74HC93 connected as a decade counter

FIGURE 9-12 2-bit synchronous binary counters.



(a) J-K flip-flop



(b) D flip-flop

FIGURE 9-13 Timing details for the 2-bit synchronous counter operation (the propagation delays of both flip-flops are assumed to be equal).

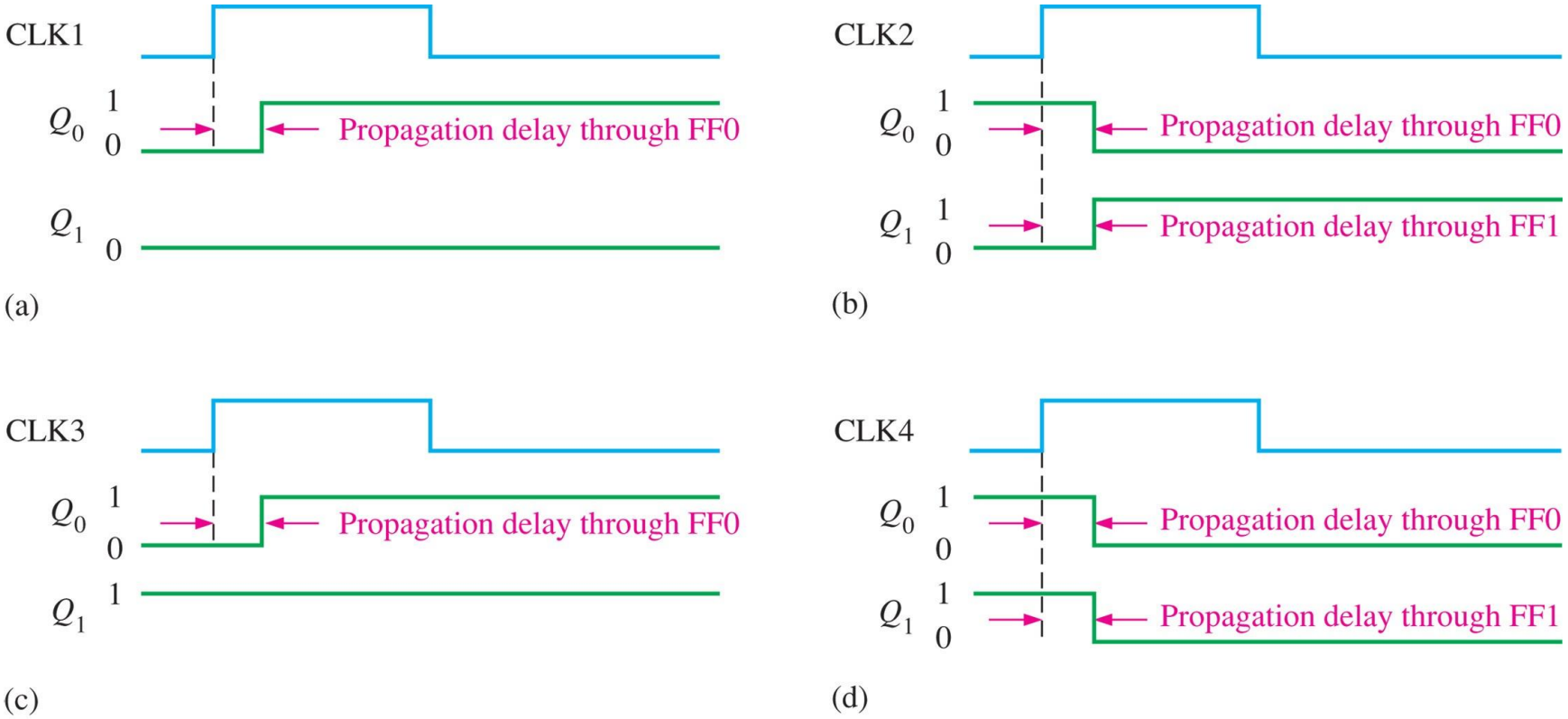
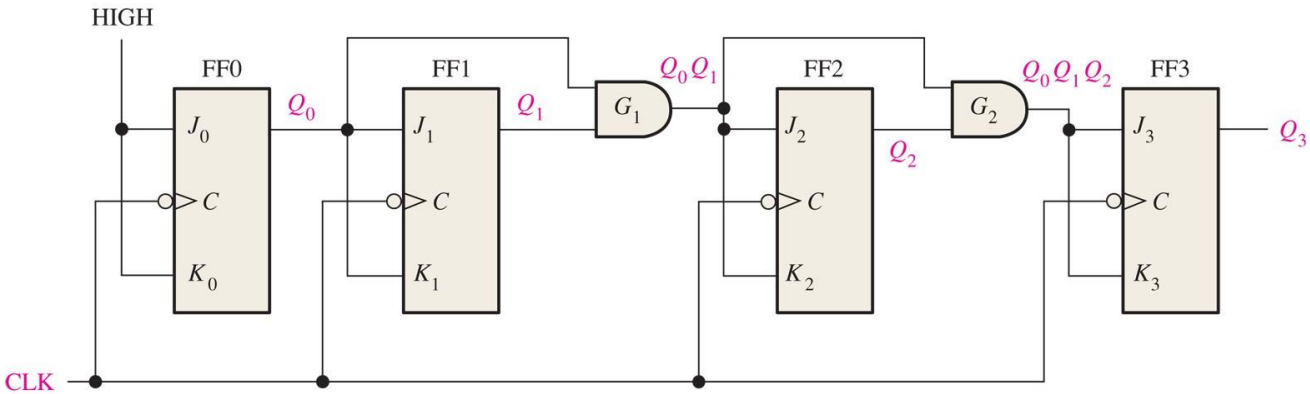
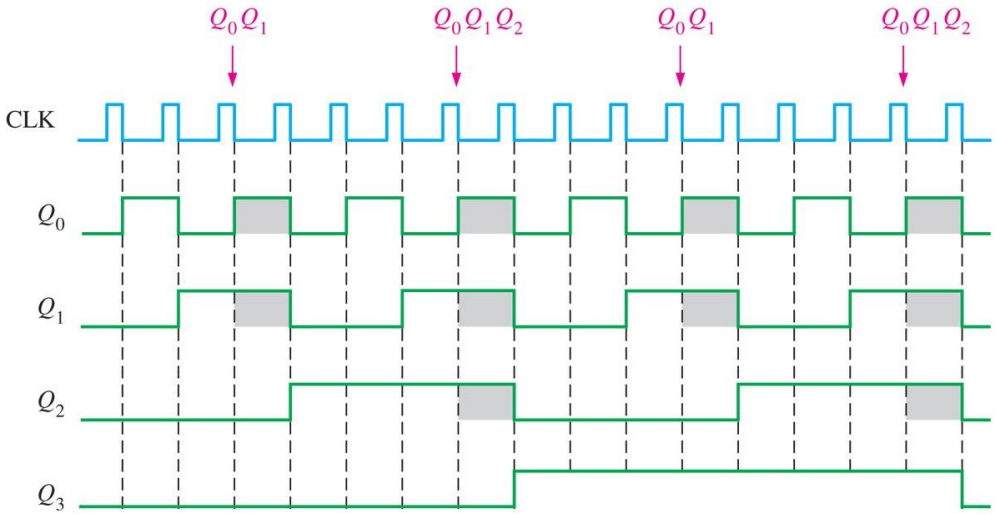


FIGURE 9-17 A 4-bit synchronous binary counter and timing diagram. Times where the AND gate outputs are HIGH are indicated by the shaded areas.



(a)



(b)

FIGURE 9-18 A synchronous BCD decade counter.

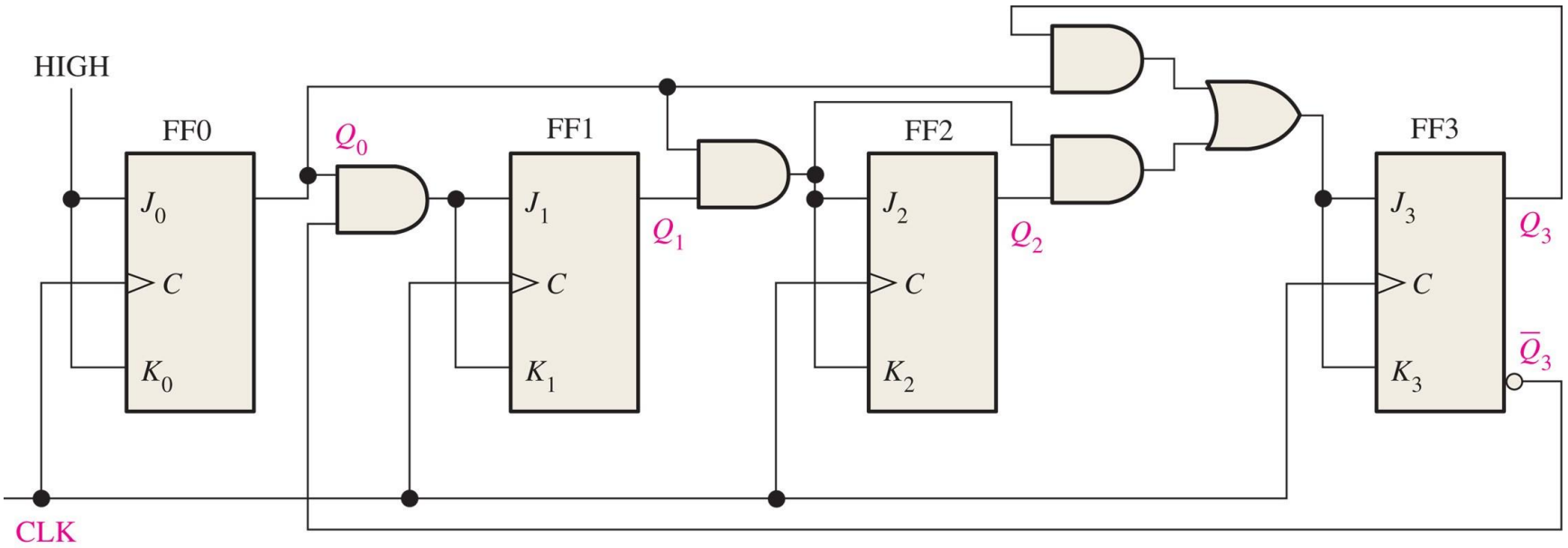


FIGURE 9-19 Timing diagram for the BCD decade counter (Q_0 is the LSB).

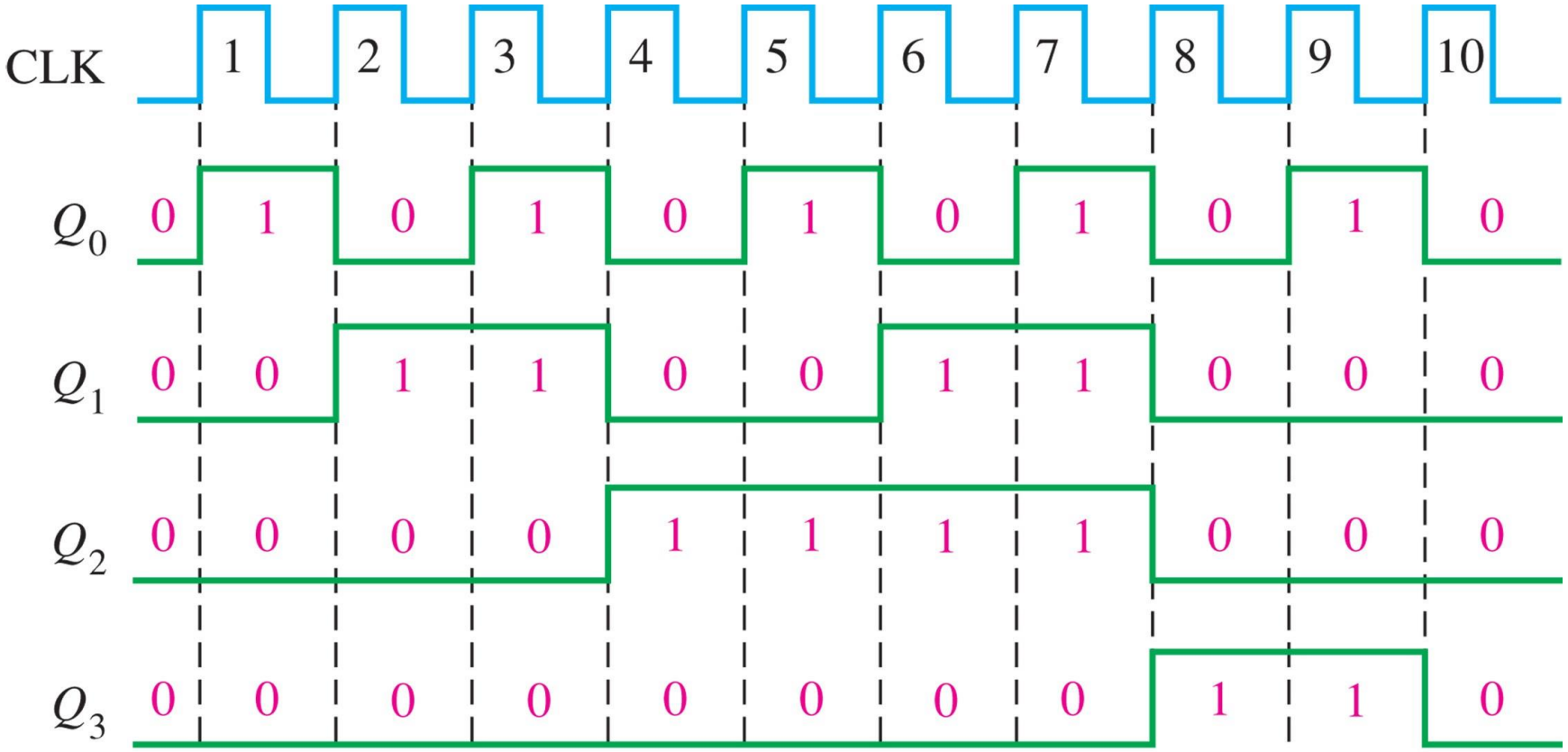


FIGURE 9-20 The 74HC163 4-bit synchronous binary counter. (The qualifying label CTR DIV 16 indicates a counter with sixteen states.)

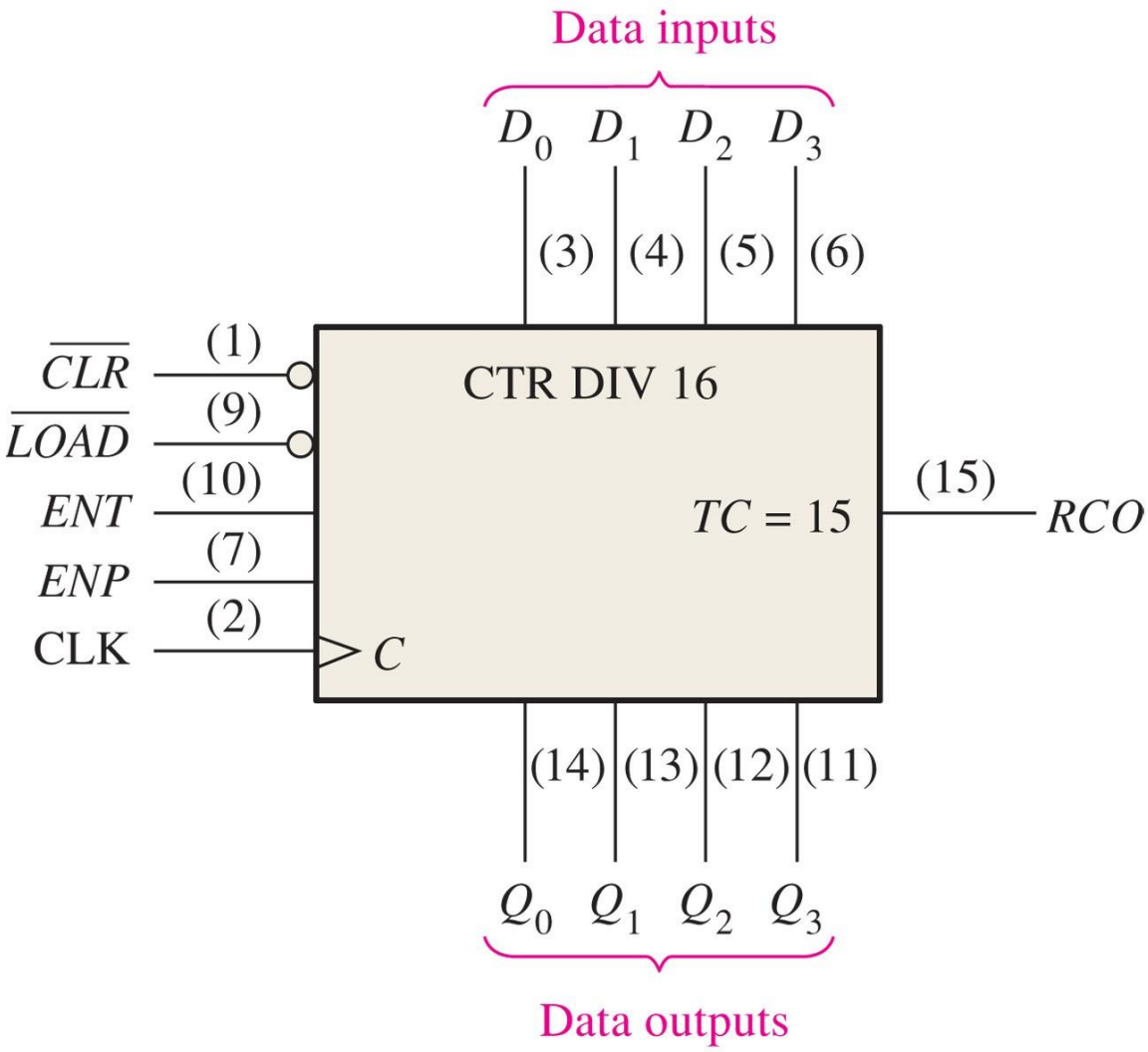


FIGURE 9-21 Timing example for a 74HC163.

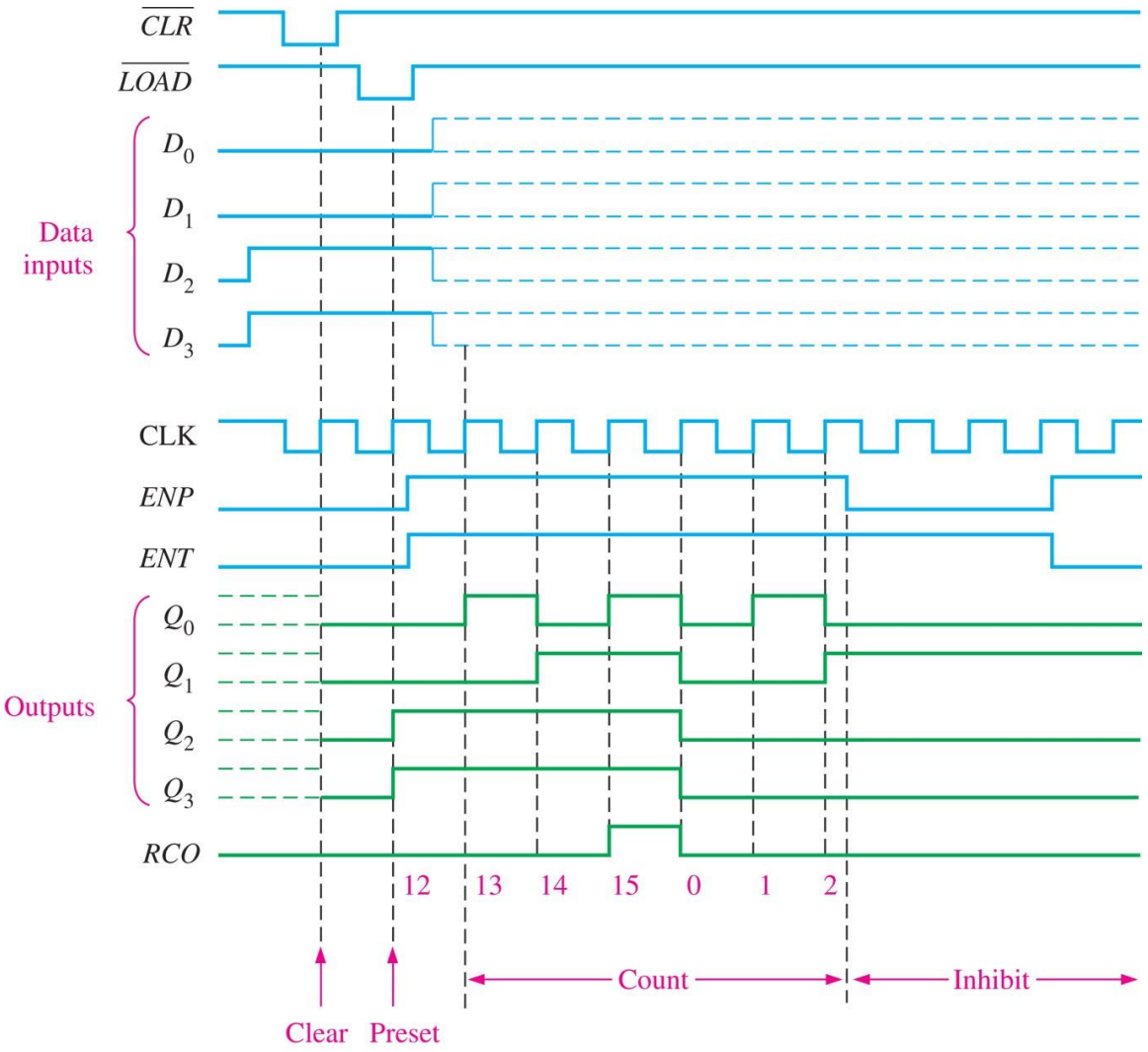


TABLE 9–6

Up/Down sequence for a 3-bit binary counter.

Clock Pulse	Up	Q_2	Q_1	Q_0	Down
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

FIGURE 9-22 A basic 3-bit up/down synchronous counter.

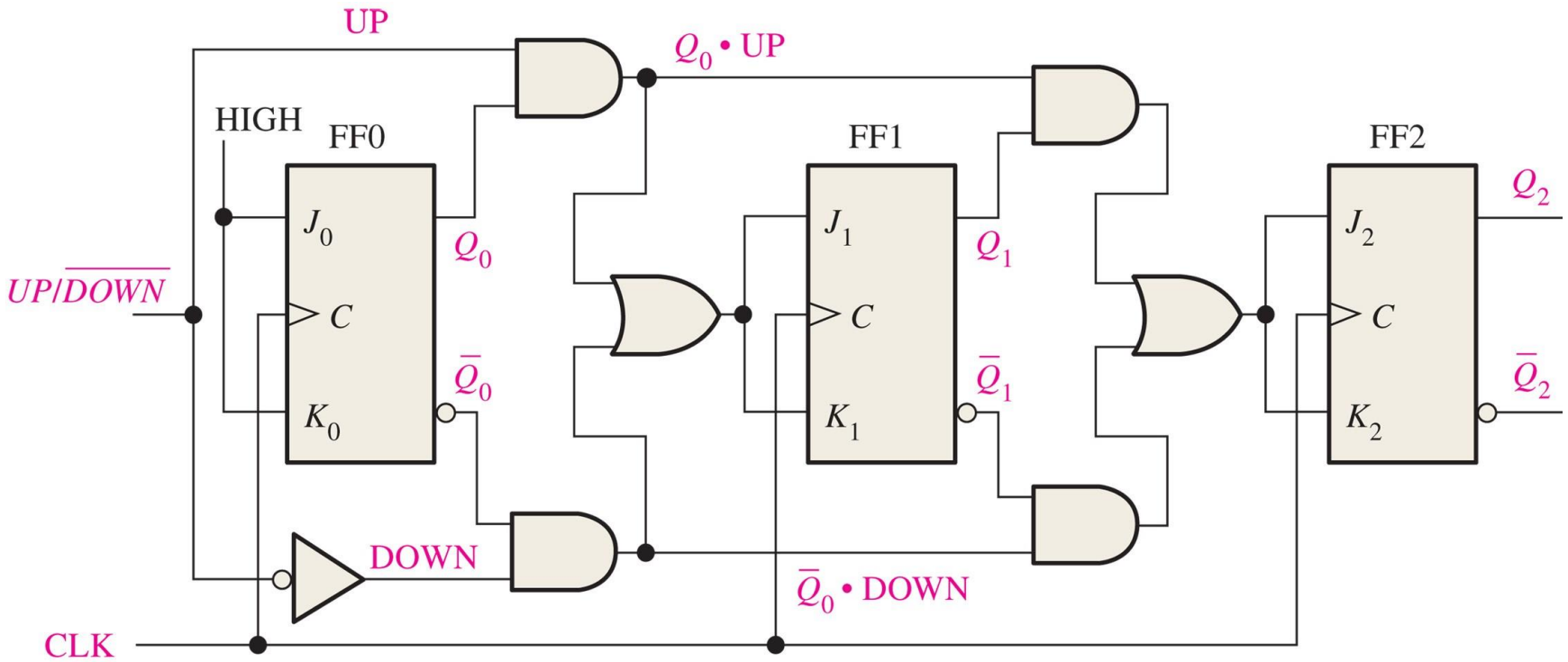


FIGURE 9-23 A 4-bit up/down counter

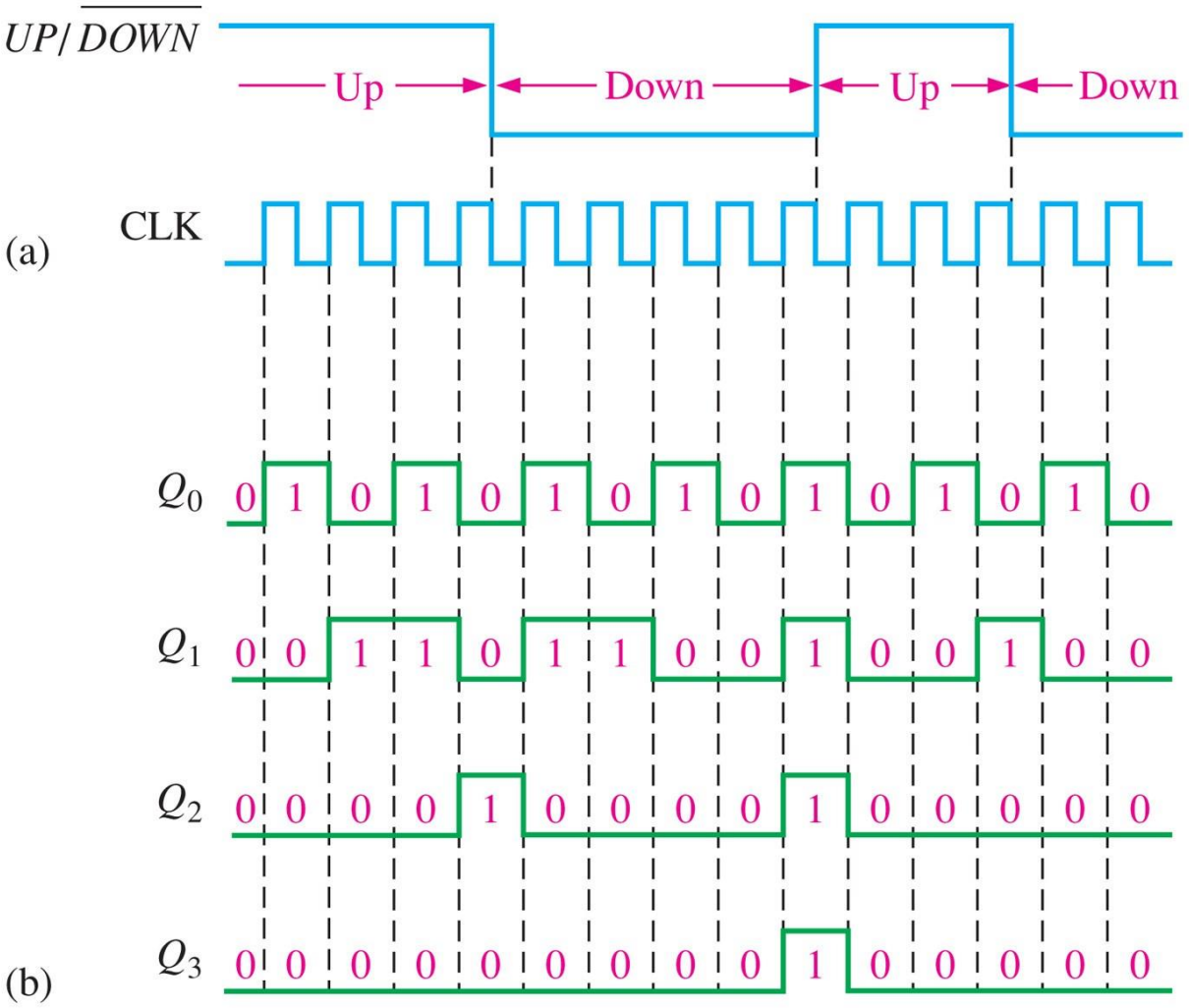


FIGURE 9-24 The 74HC190 up/down synchronous decade counter.

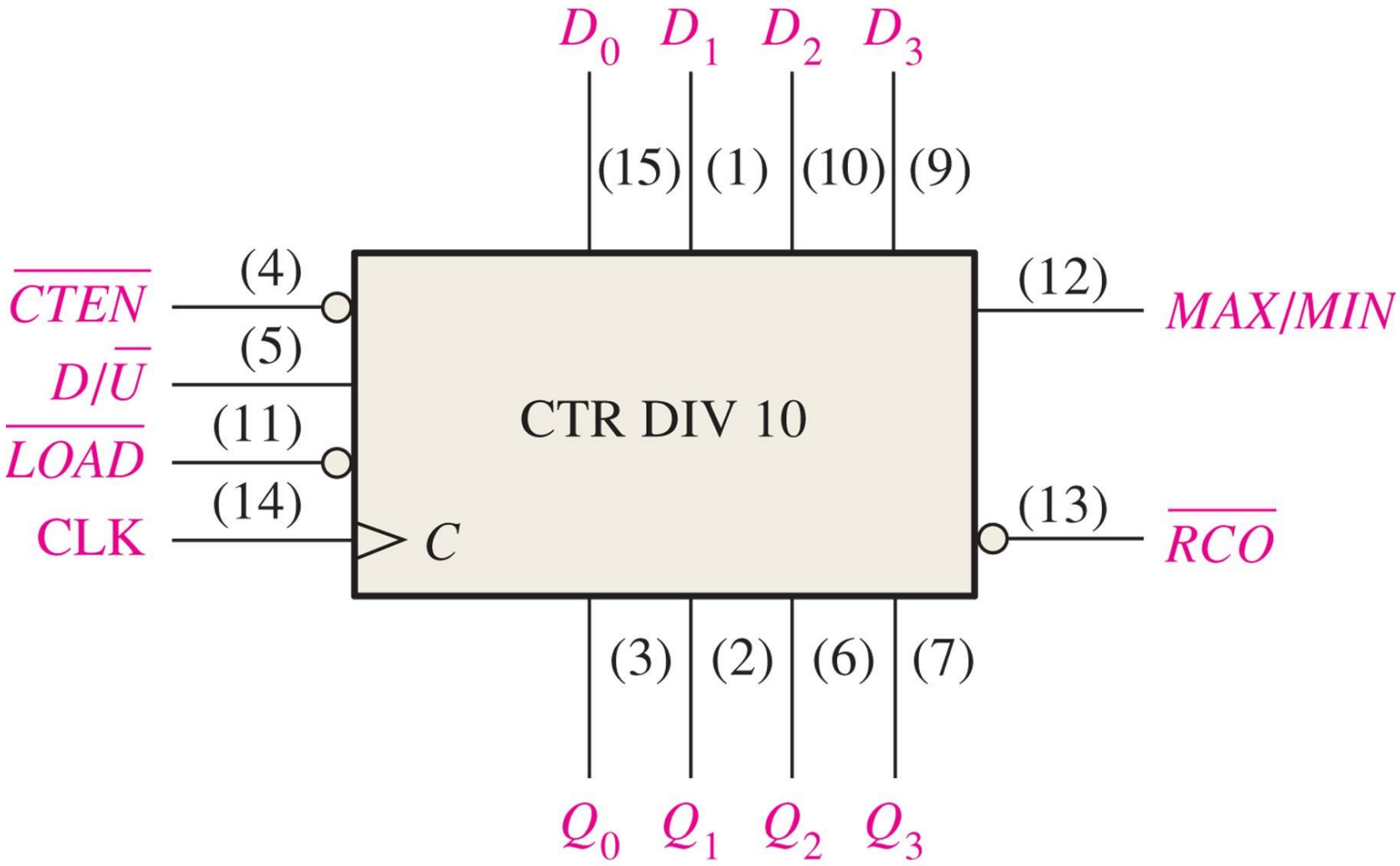


FIGURE 9-25 Timing example for a 74HC190.

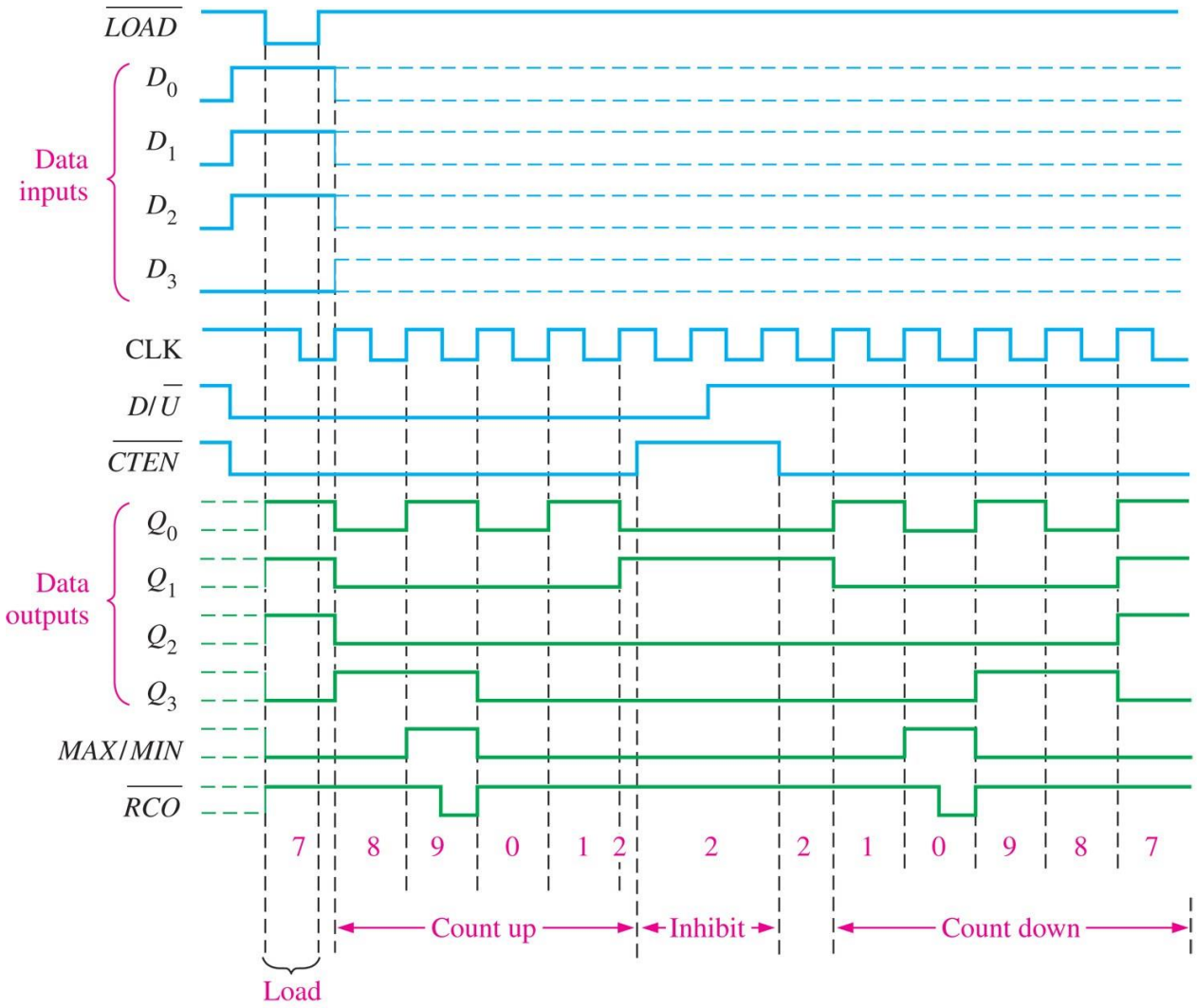


FIGURE 9-26 Karnaugh map example: State diagram for a 3-bit Gray code counter.

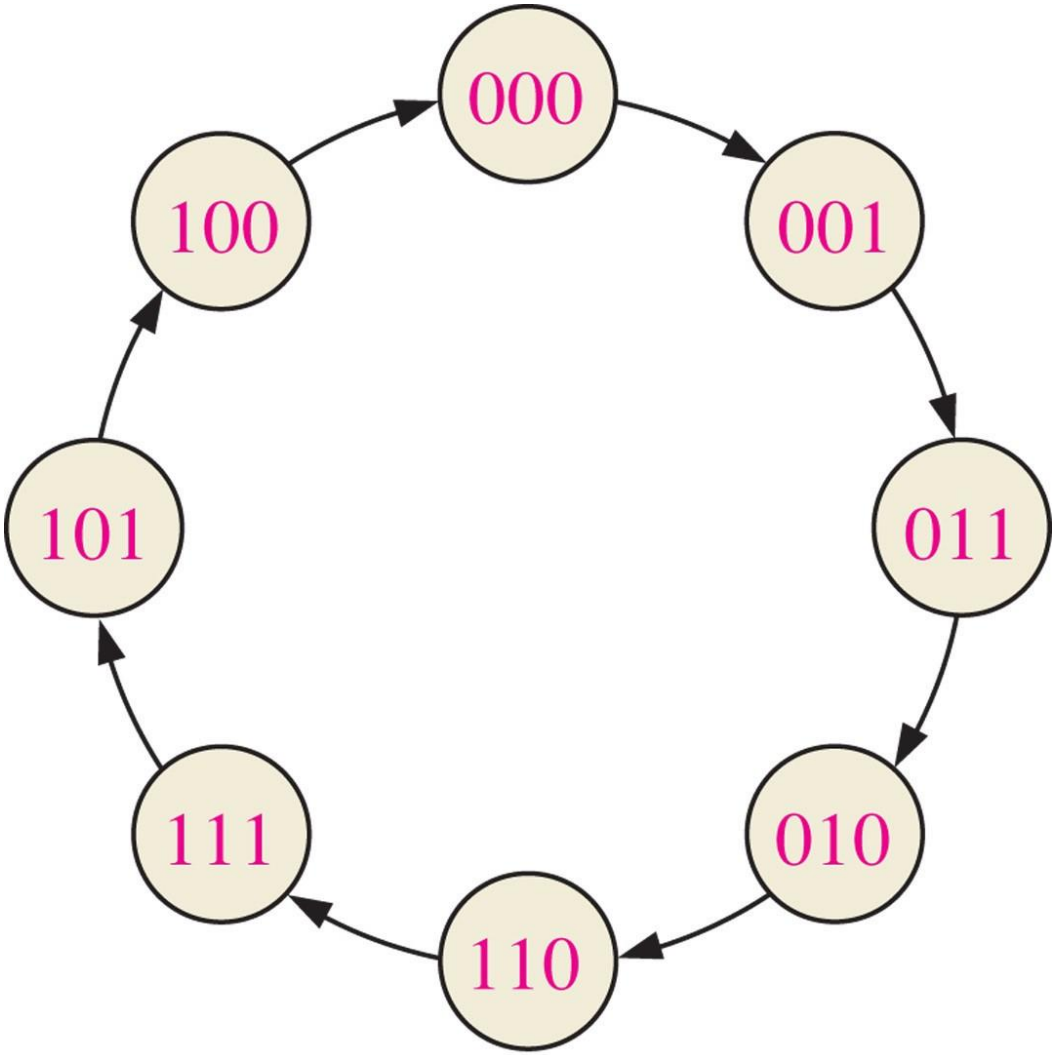


TABLE 9–9

Transition table for a J-K flip-flop.

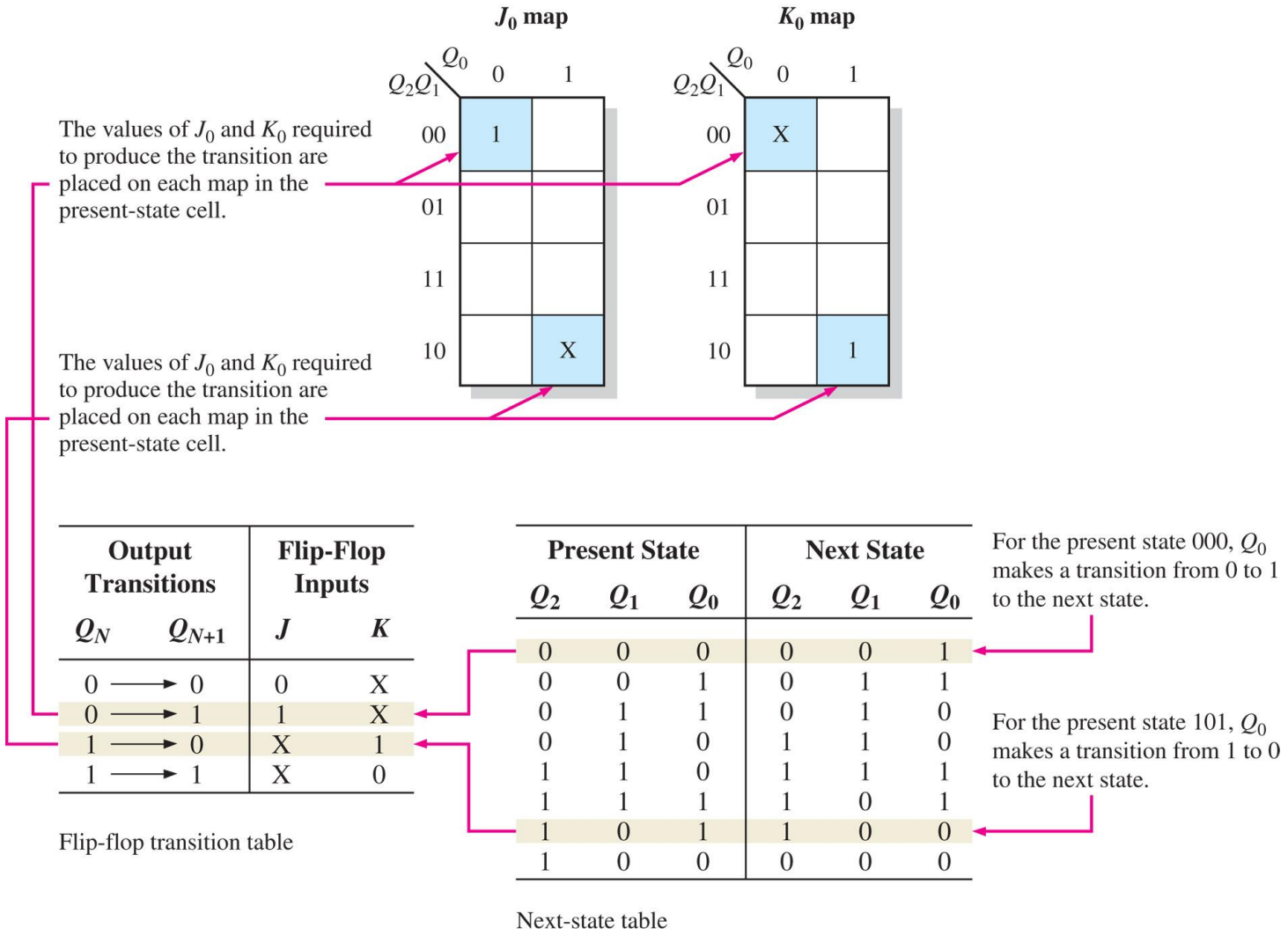
Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Q_N: present state

Q_{N+1}: next state

X: "don't care"

FIGURE 9-27 Examples of the mapping procedure for the counter sequence represented in Table 9–8 and Table 9–9.



Output Transitions		Flip-Flop Inputs	
Q_N	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Flip-flop transition table

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

For the present state 000, Q_0 makes a transition from 0 to 1 to the next state.

For the present state 101, Q_0 makes a transition from 1 to 0 to the next state.

Next-state table

FIGURE 9-28 Karnaugh maps for present-state *J* and *K* inputs.

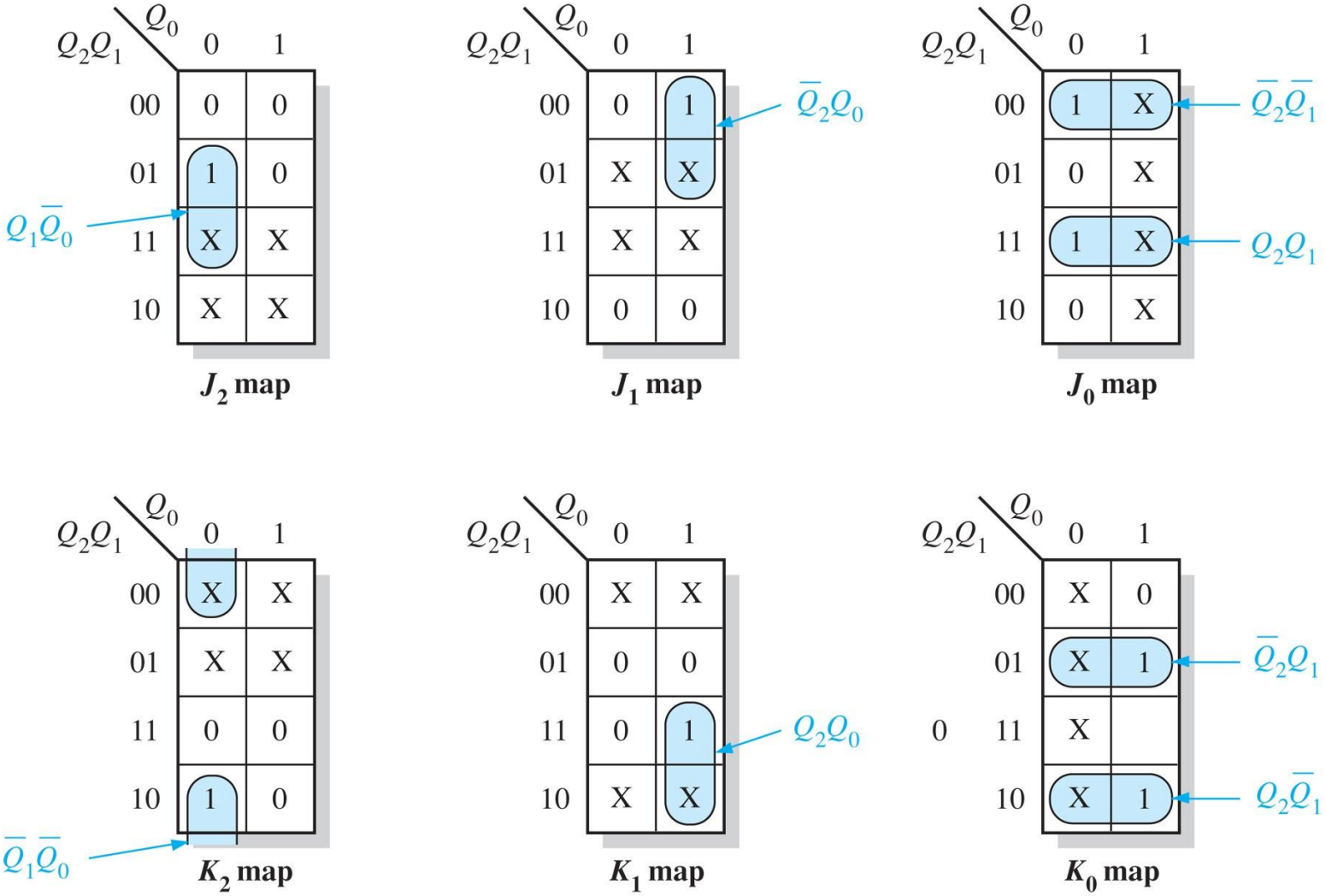


FIGURE 9-29 Three-bit Gray code counter.

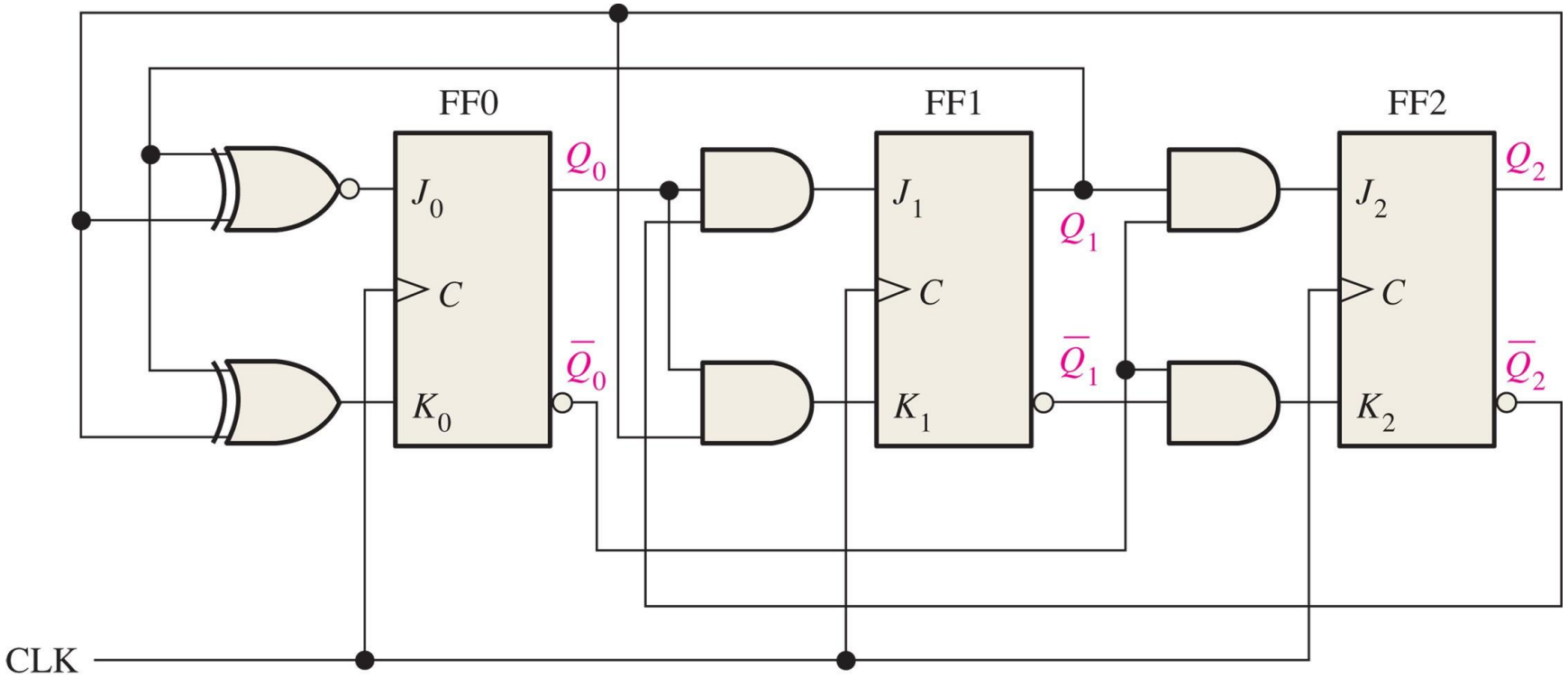


FIGURE 9-37 A modulus-100 counter using two cascaded decade counters.

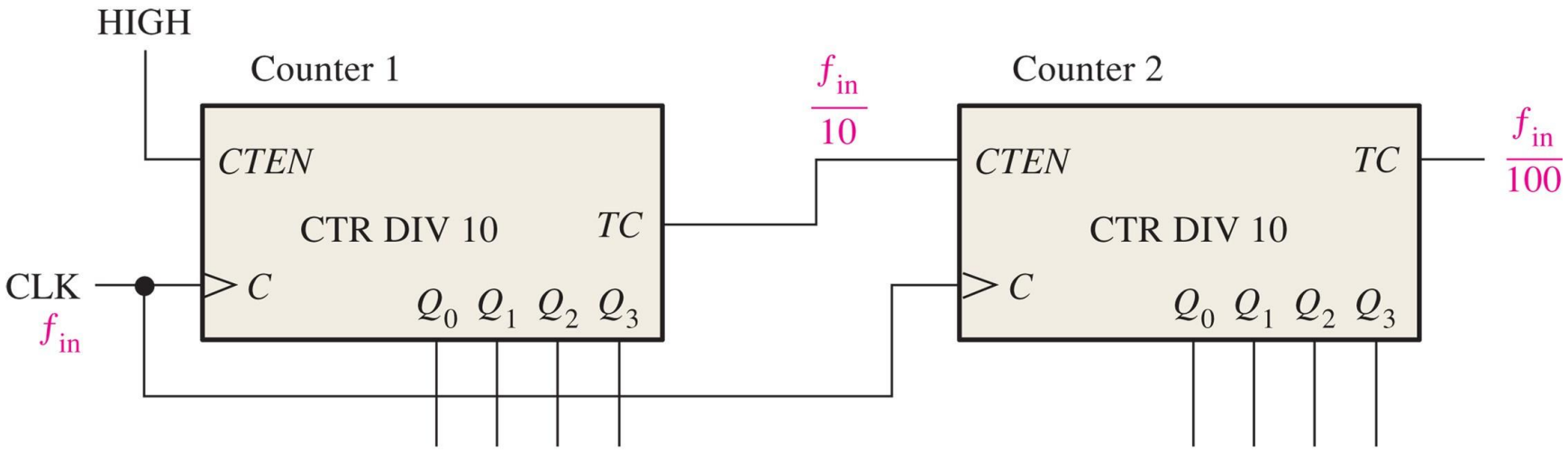


FIGURE 9-43 A 3-bit counter with active-HIGH decoding of count 2 and count 7.

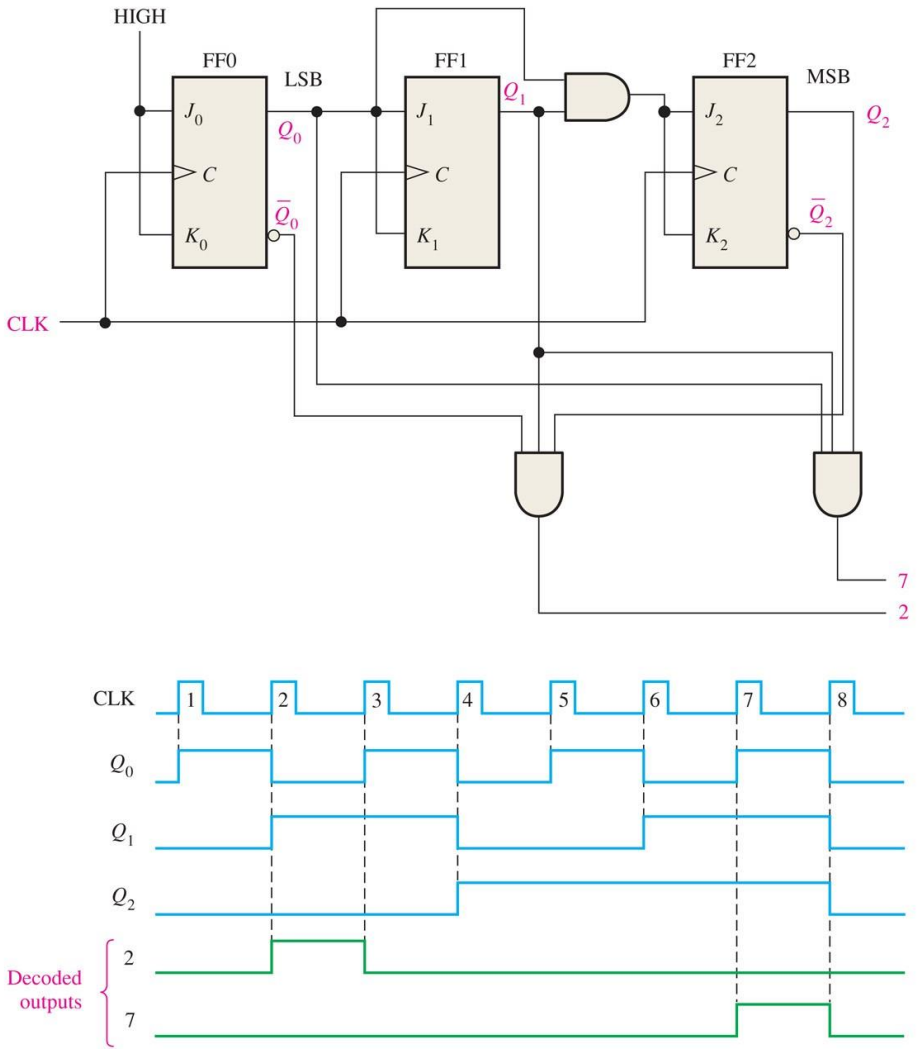


FIGURE 9-44 A basic decade (BCD) counter and decoder.

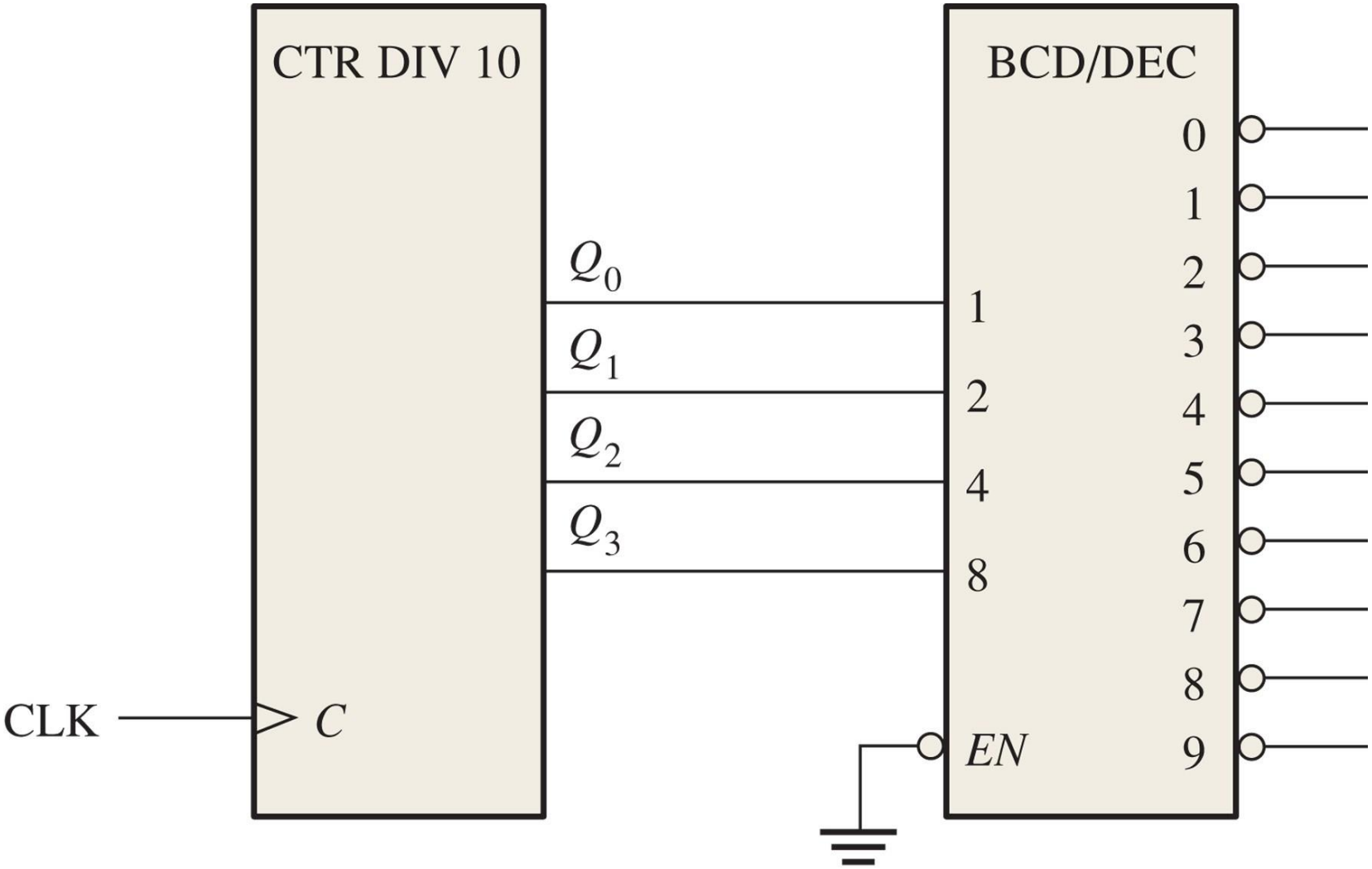


FIGURE 9-45 Outputs with glitches from the decoder in Figure 9-44. Glitch widths are exaggerated for illustration and are usually only a few nanoseconds wide.

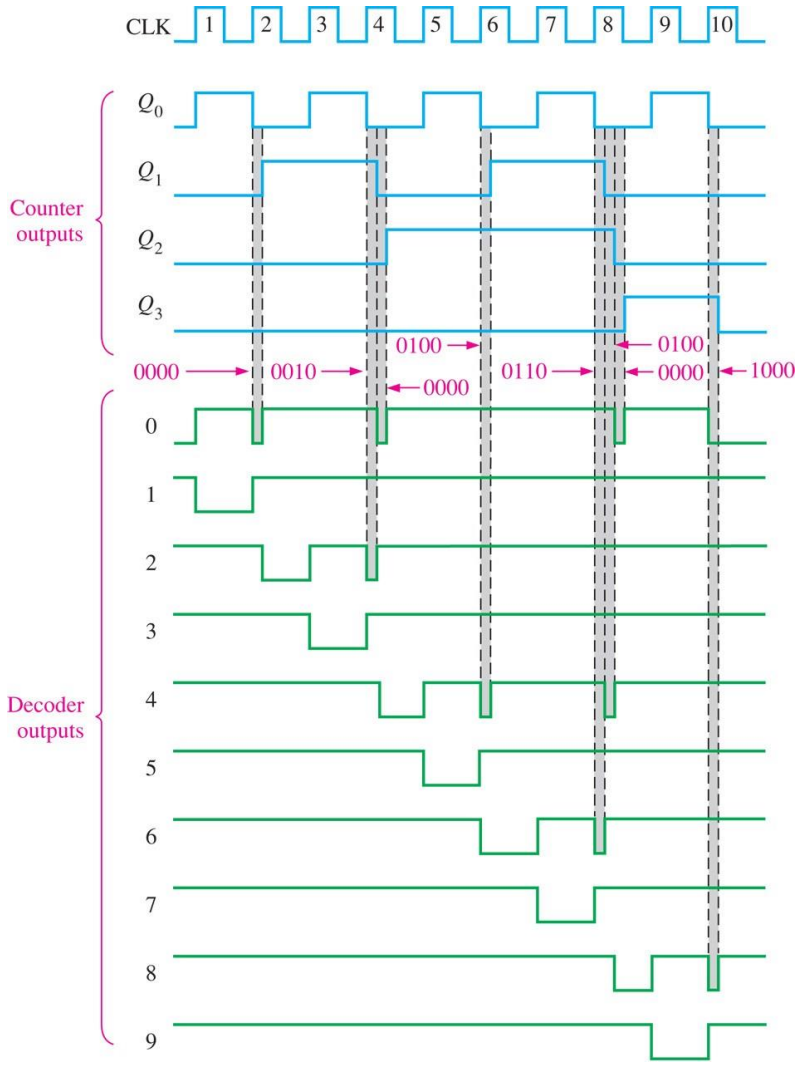


FIGURE 9-46 The basic decade counter and decoder with strobing to eliminate glitches.

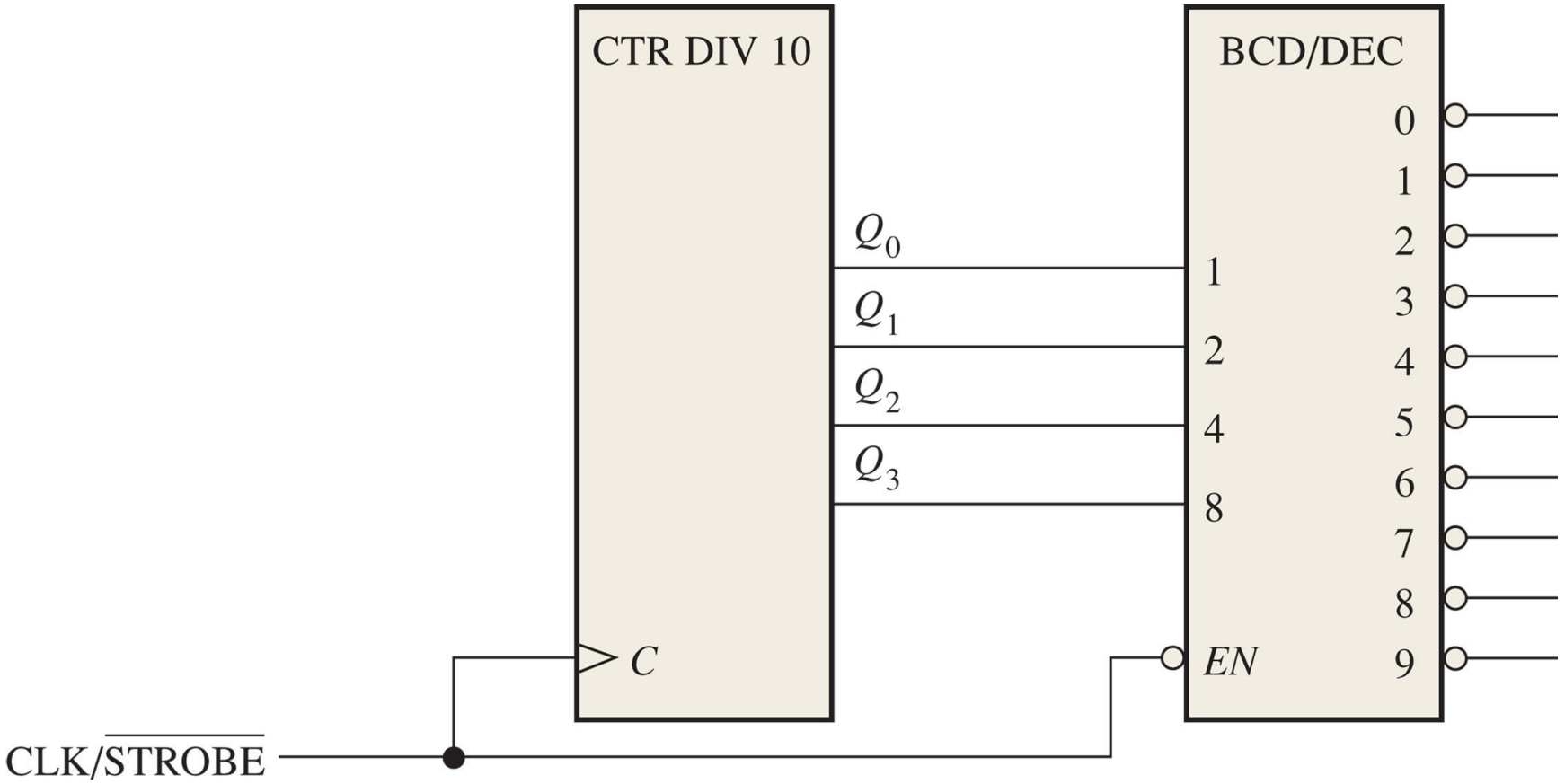


FIGURE 9-47 Strobed decoder outputs for the circuit of Figure 9-46.

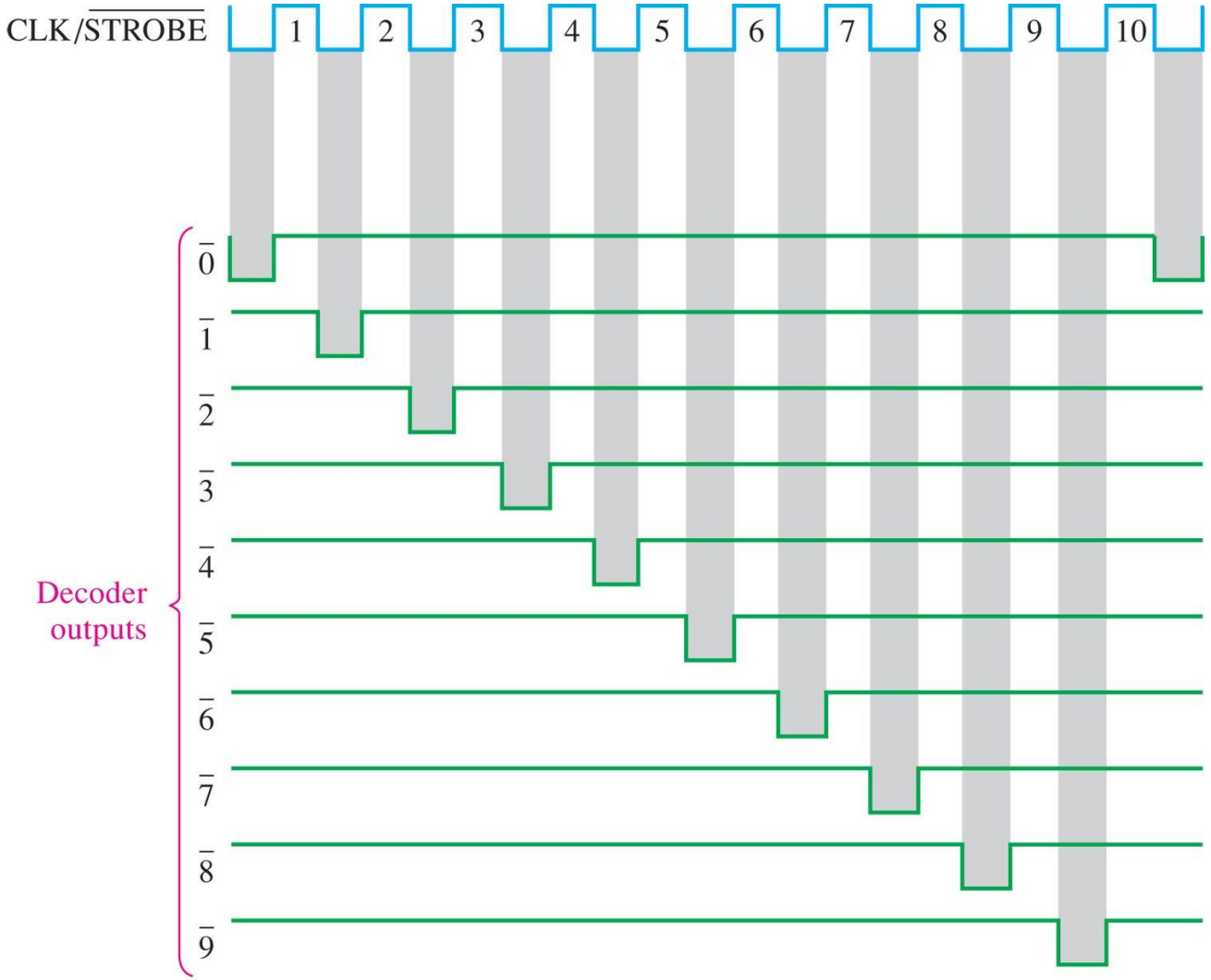


FIGURE 9-48 Simplified logic diagram for a 12-hour digital clock. Logic details using specific devices are shown in Figures 9-49 and 9-50.

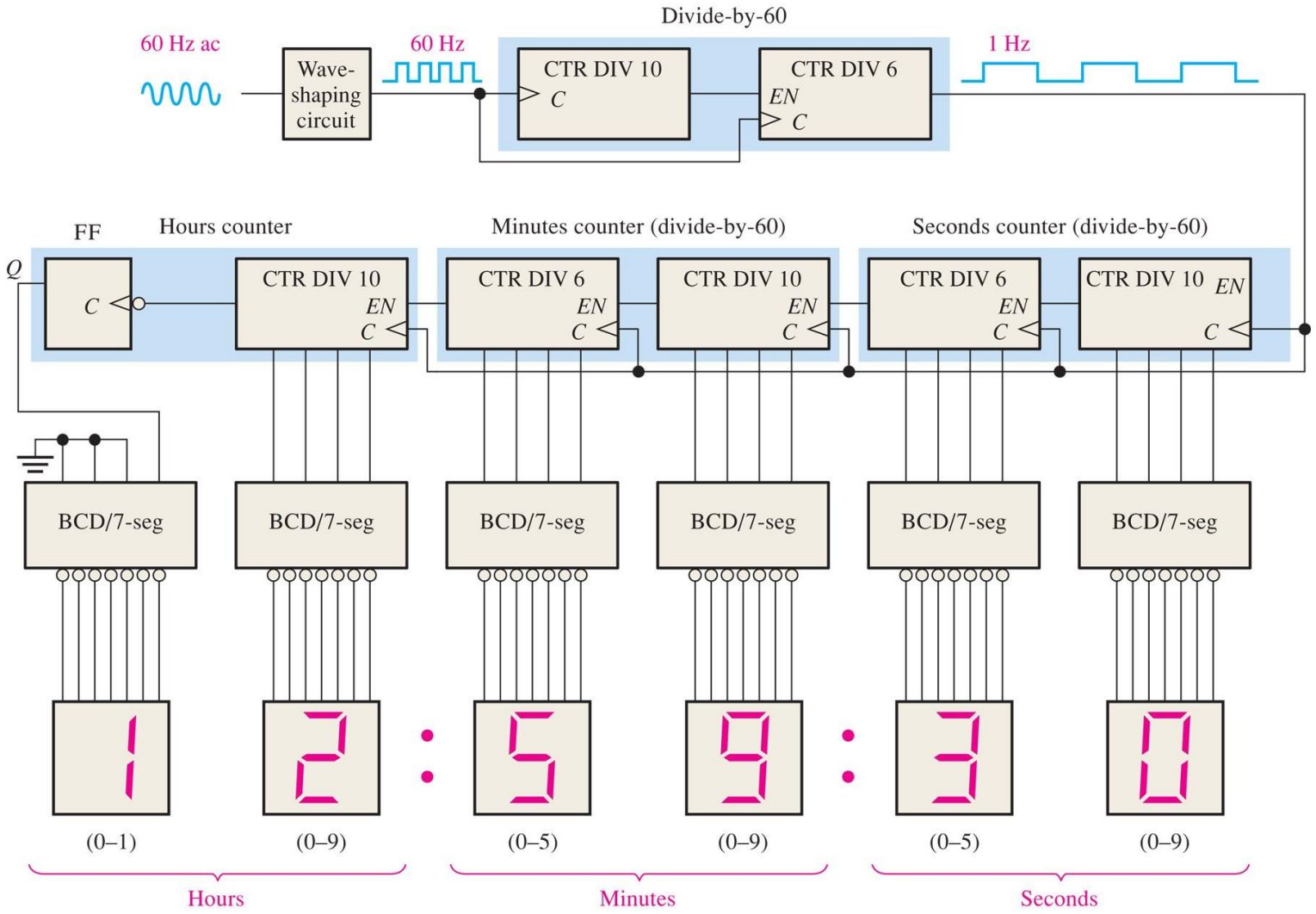


FIGURE 9-50 GS Logic diagram for hours counter and decoders. Note that on the counter inputs and outputs, the right-most bit is the LSB.

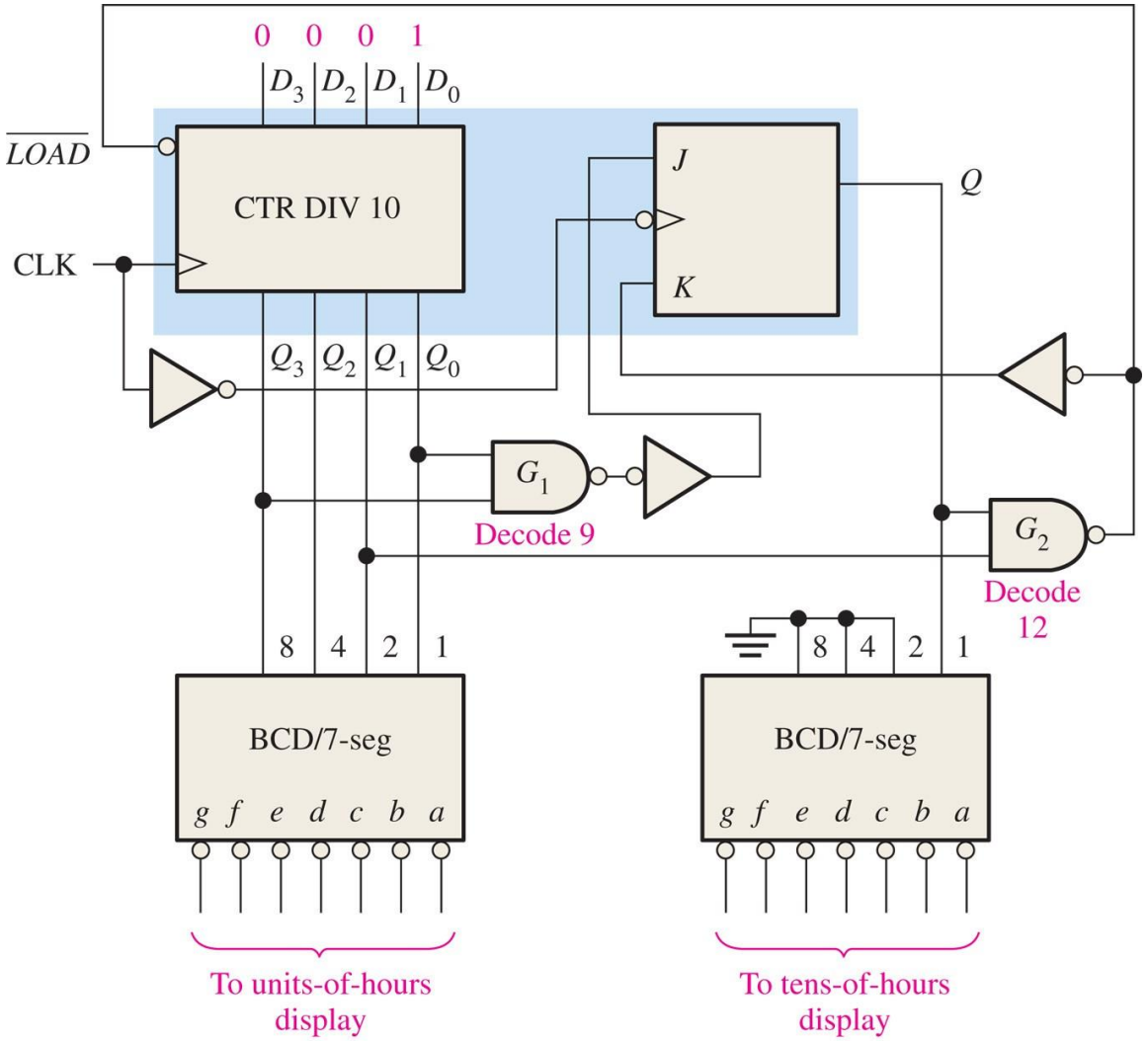


FIGURE 9-51 Functional block diagram for parking garage control.

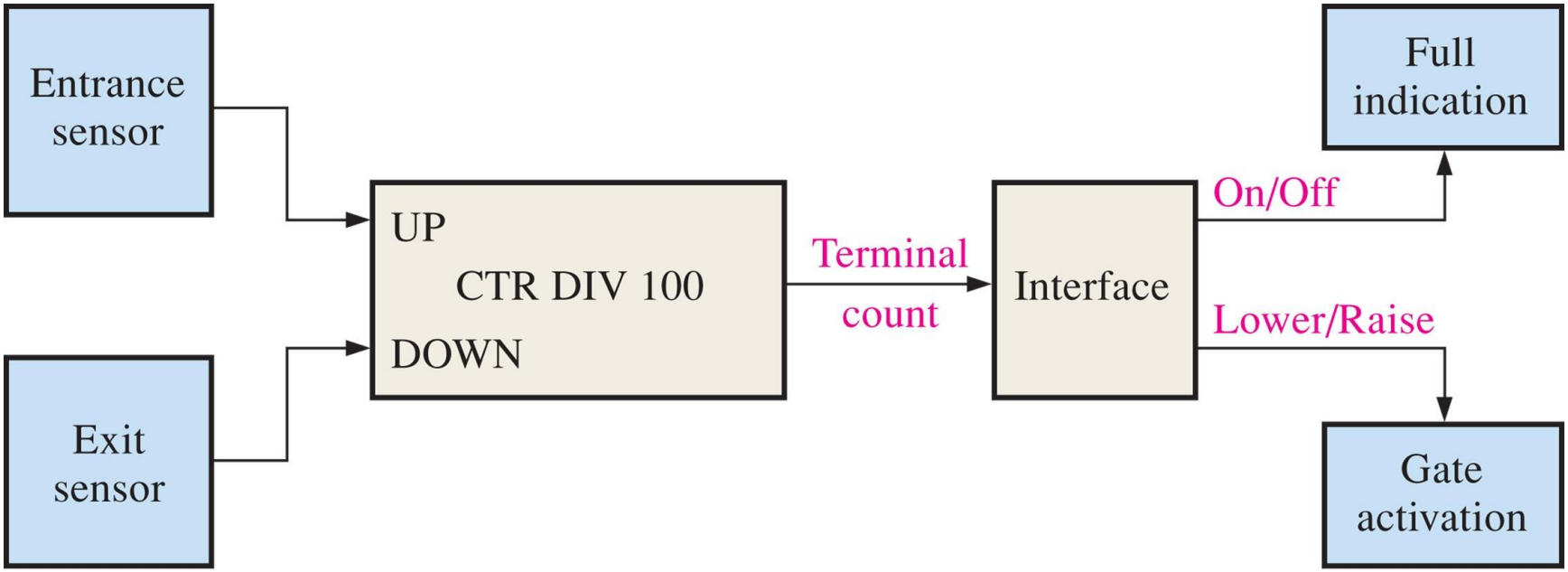


FIGURE 9-52 Logic diagram for modulus-100 up/down counter for automobile parking control.

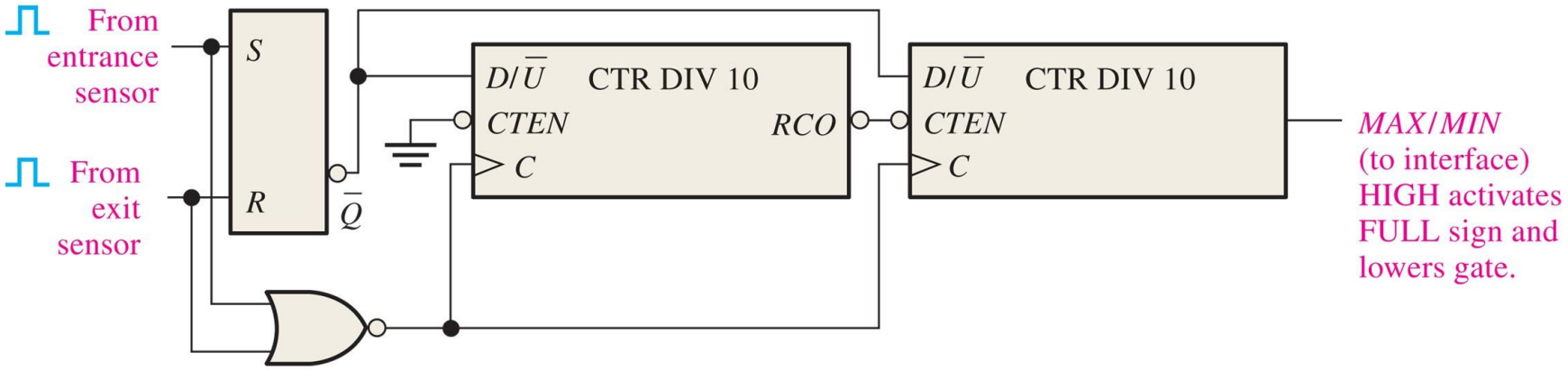


FIGURE 9-53 Parallel-to-serial data conversion logic.

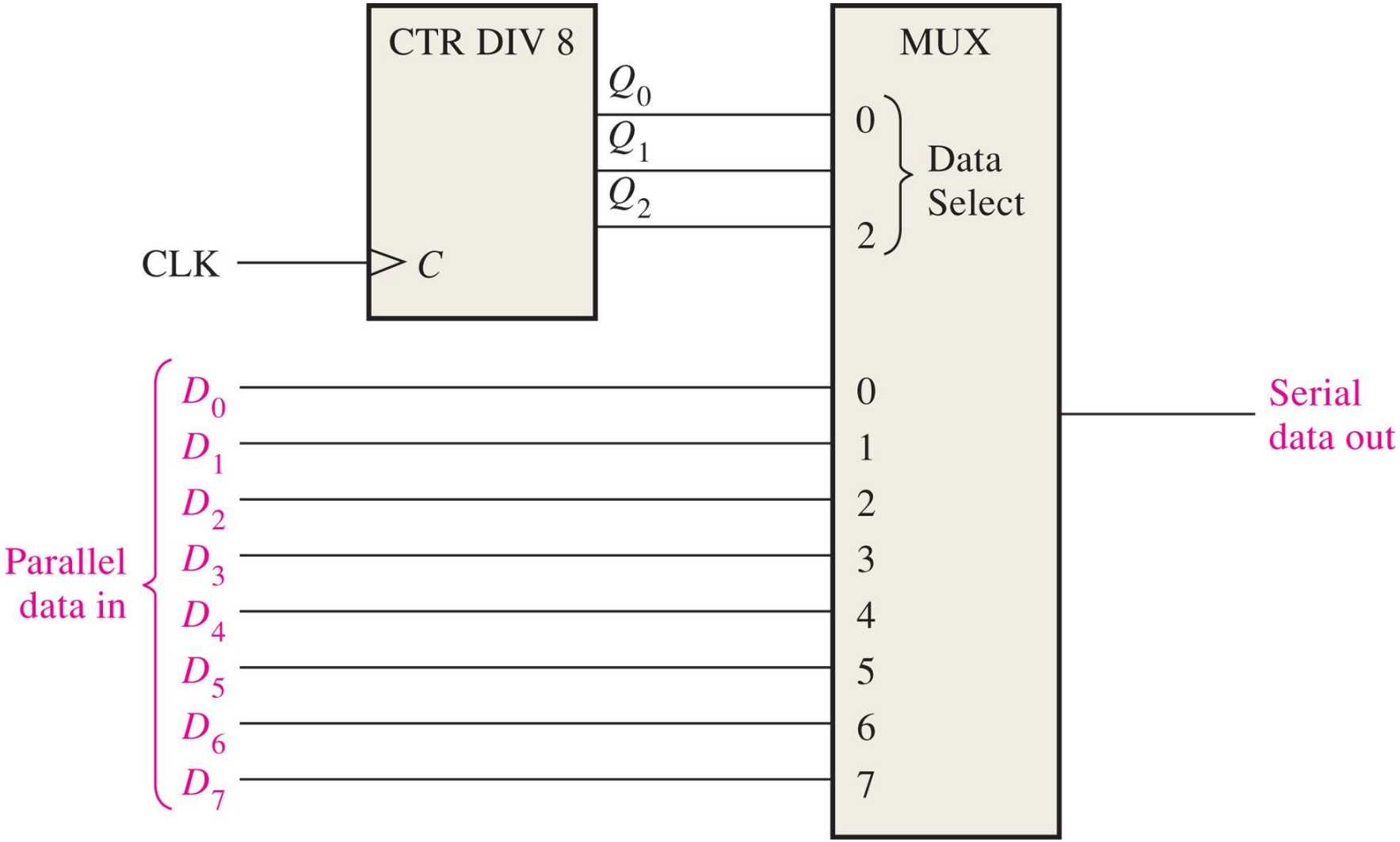


FIGURE 9-54 Example of parallel-to-serial conversion timing for the circuit in Figure 9-53.

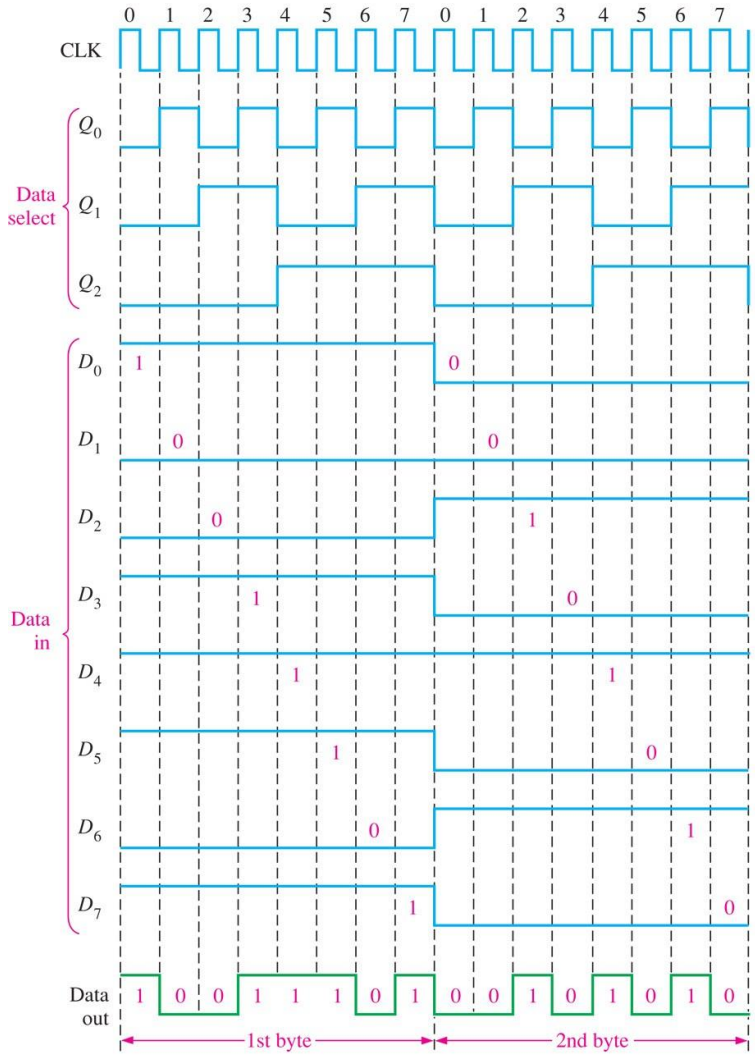
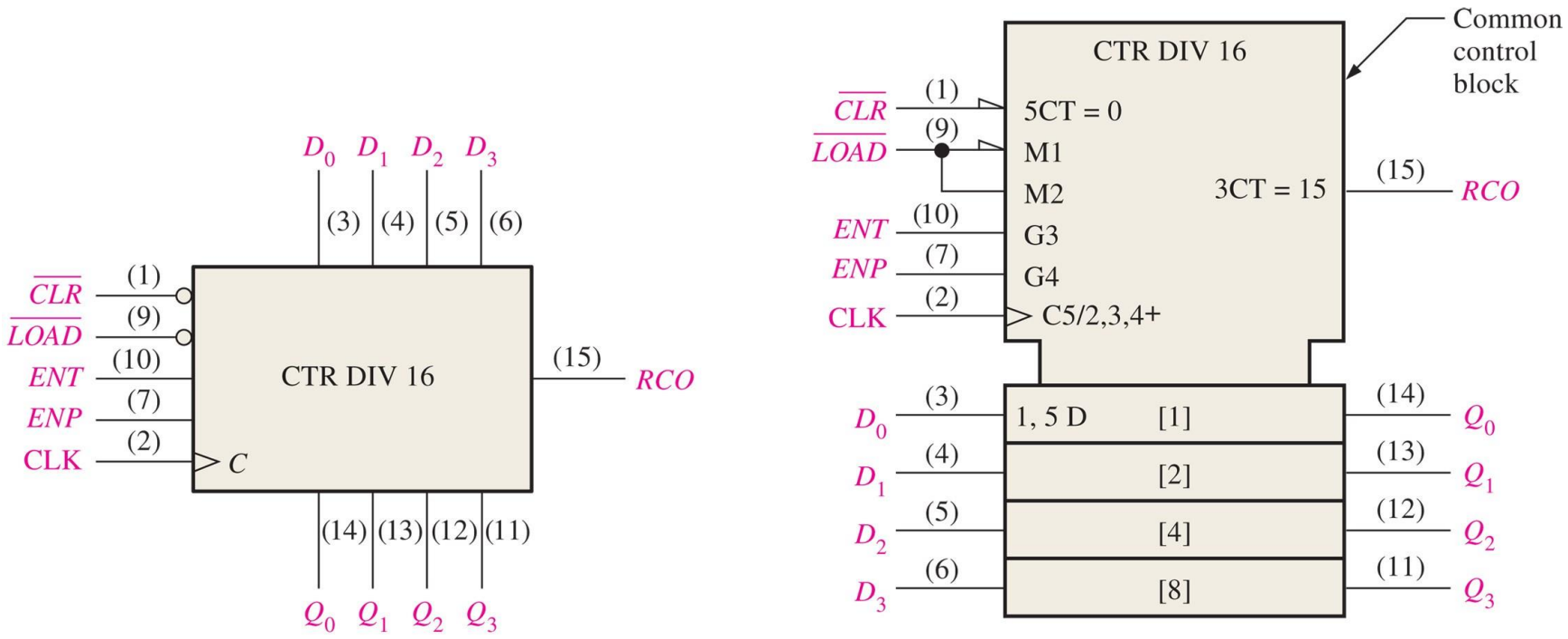


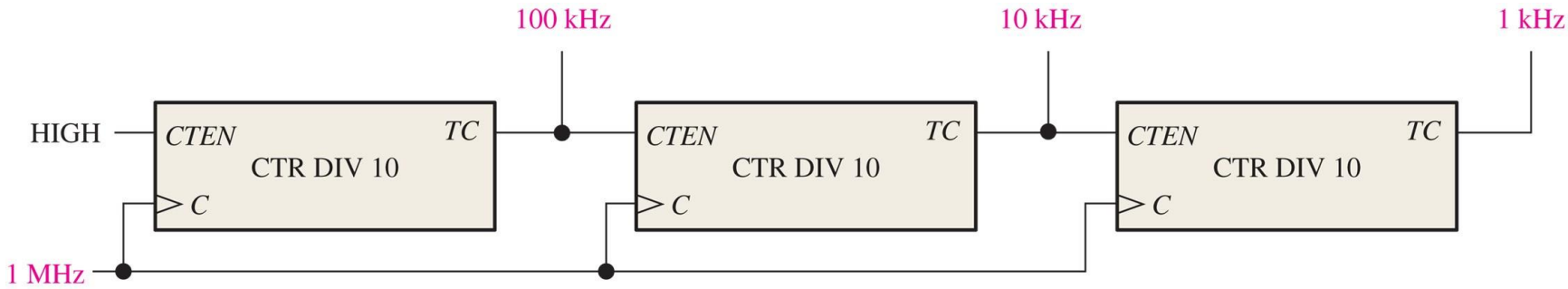
FIGURE 9-55 The 74HC163 4-bit synchronous counter.



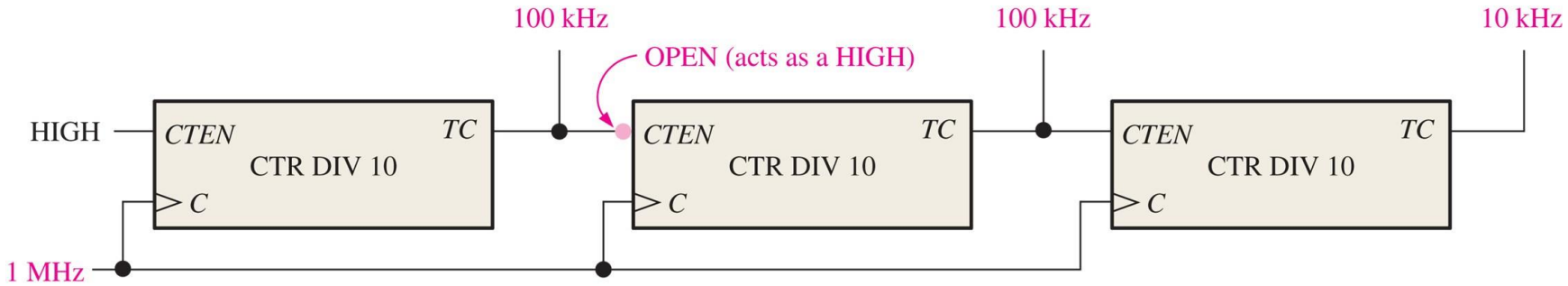
(a) Traditional block symbol

(b) ANSI/IEEE Std. 91-1984 logic symbol

FIGURE 9-56 Example of a failure that affects following counters in a cascaded arrangement.



(a) Normal operation



(b) Count Enable (*CTEN*) input of second counter open

FIGURE 9-57 Example of a failure in a cascaded counter with a truncated sequence.

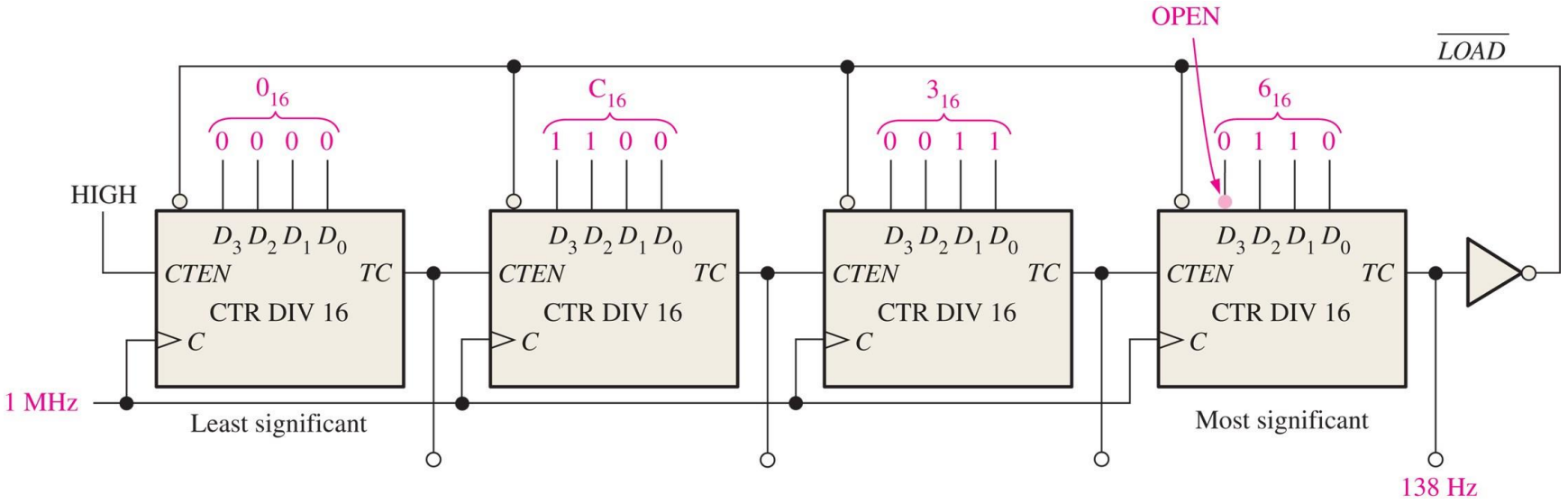


FIGURE 9-60 One cycle of the elevator operation.

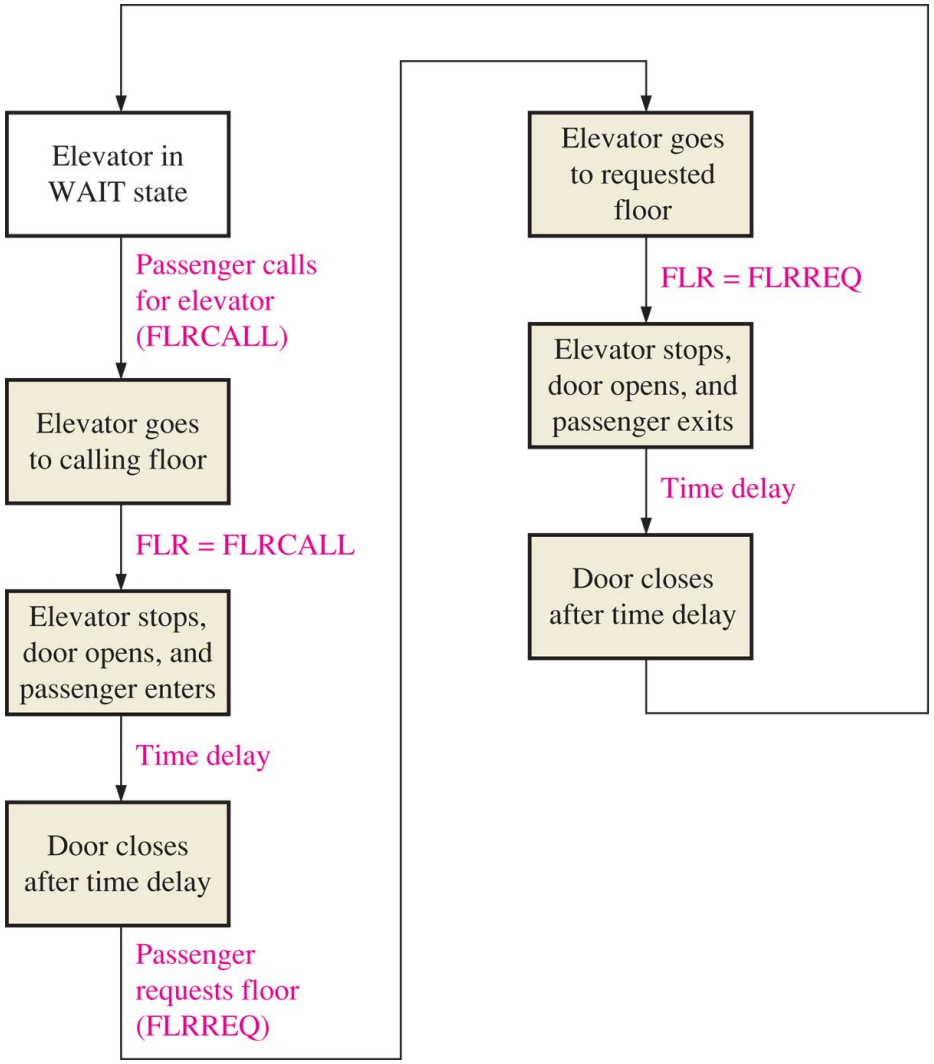


FIGURE 9-61 Elevator controller state diagram.

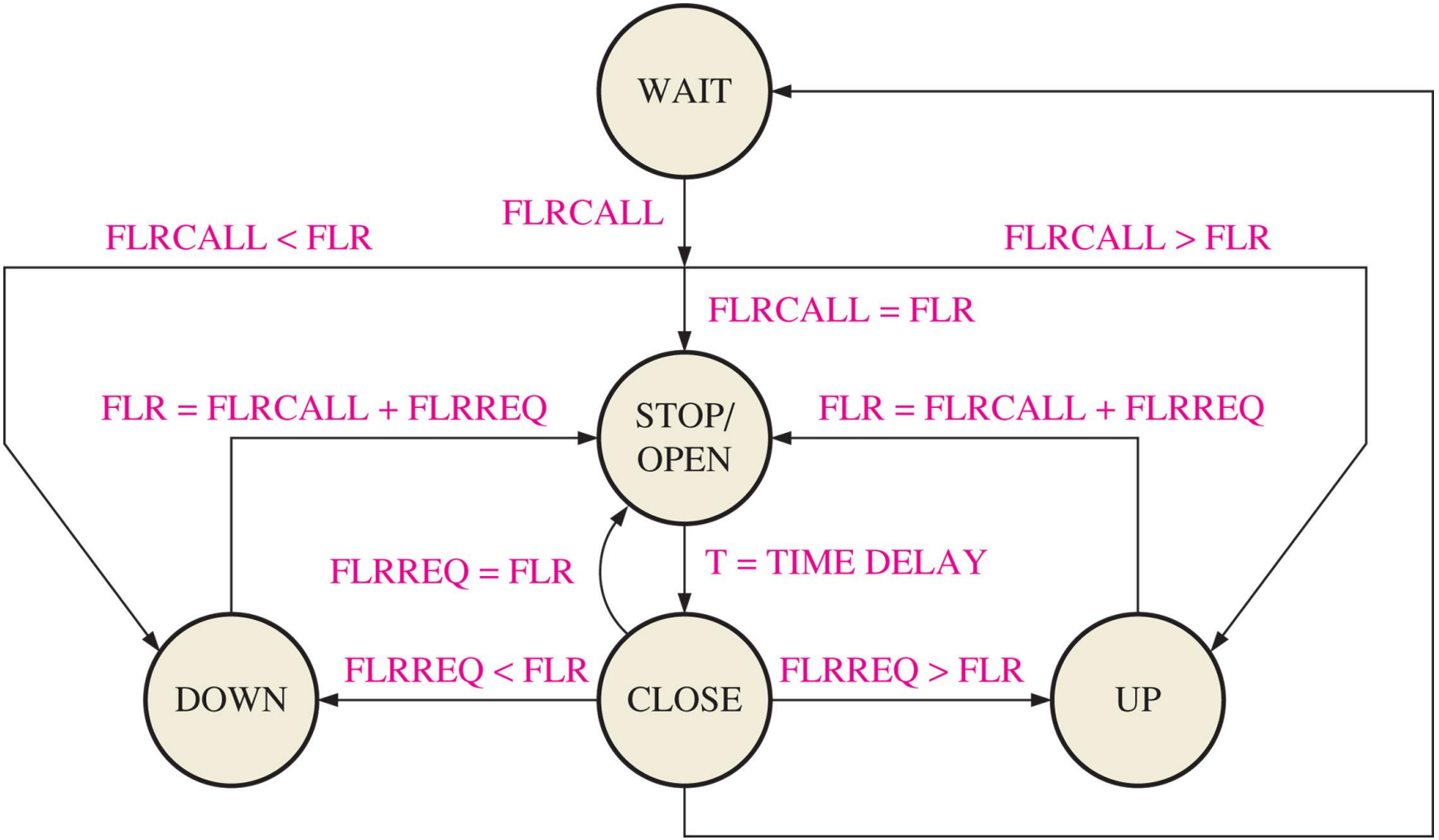


FIGURE 9-62 Elevator controller block diagram.

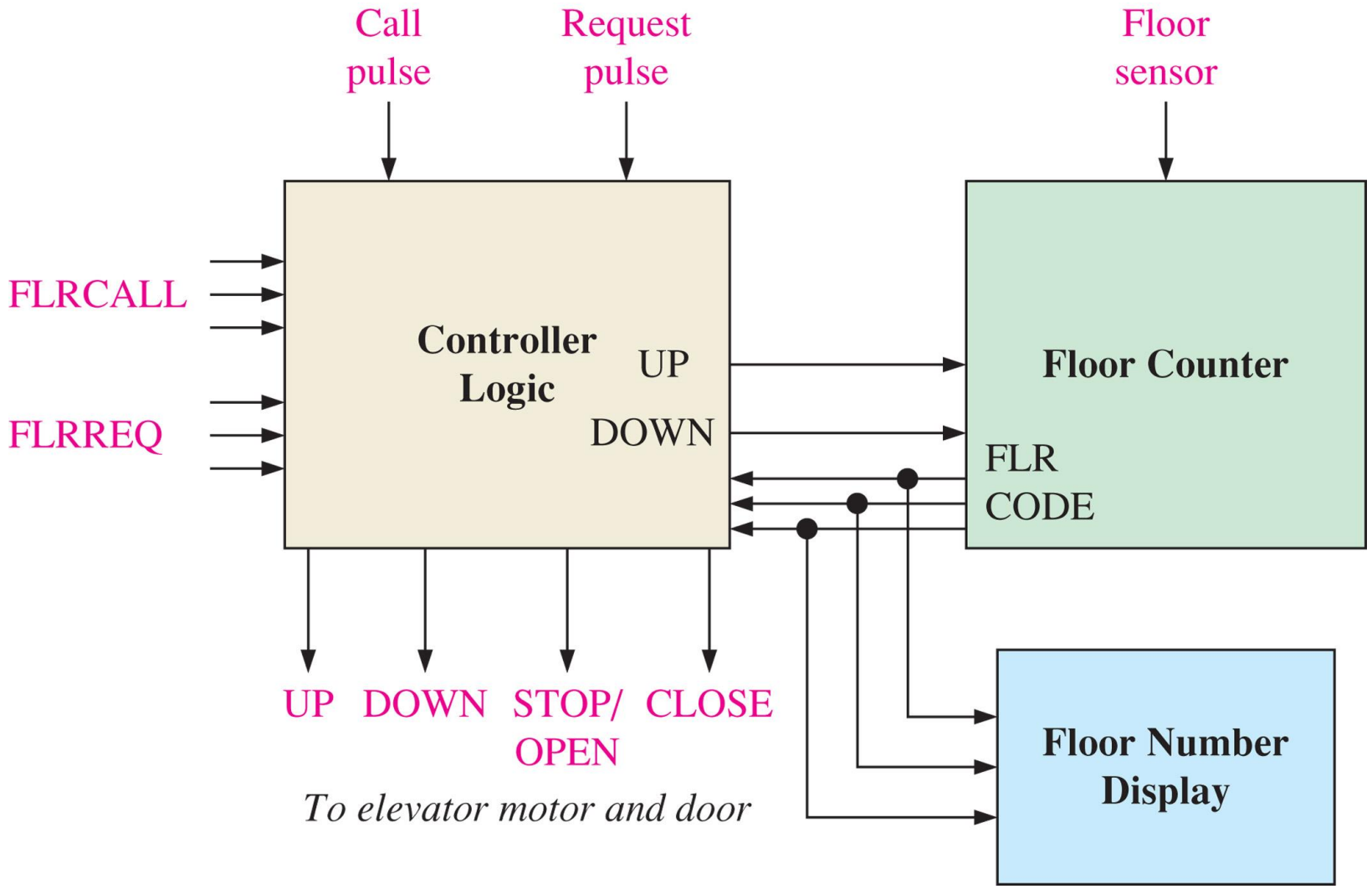


FIGURE 9-63 Floor counter state diagram.

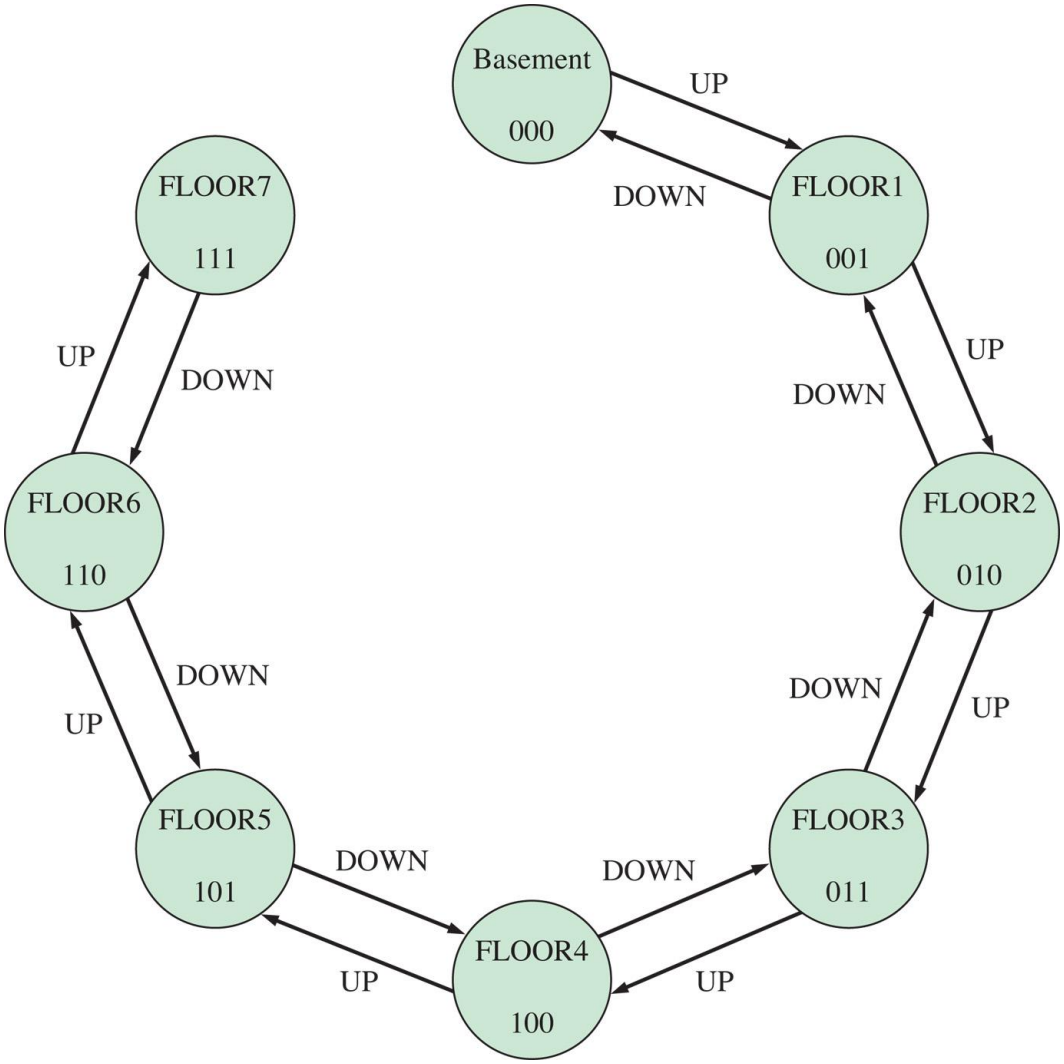


FIGURE 9-64 Elevator controller logic diagram.