Electronics II – Chapter 3

Logic Gates

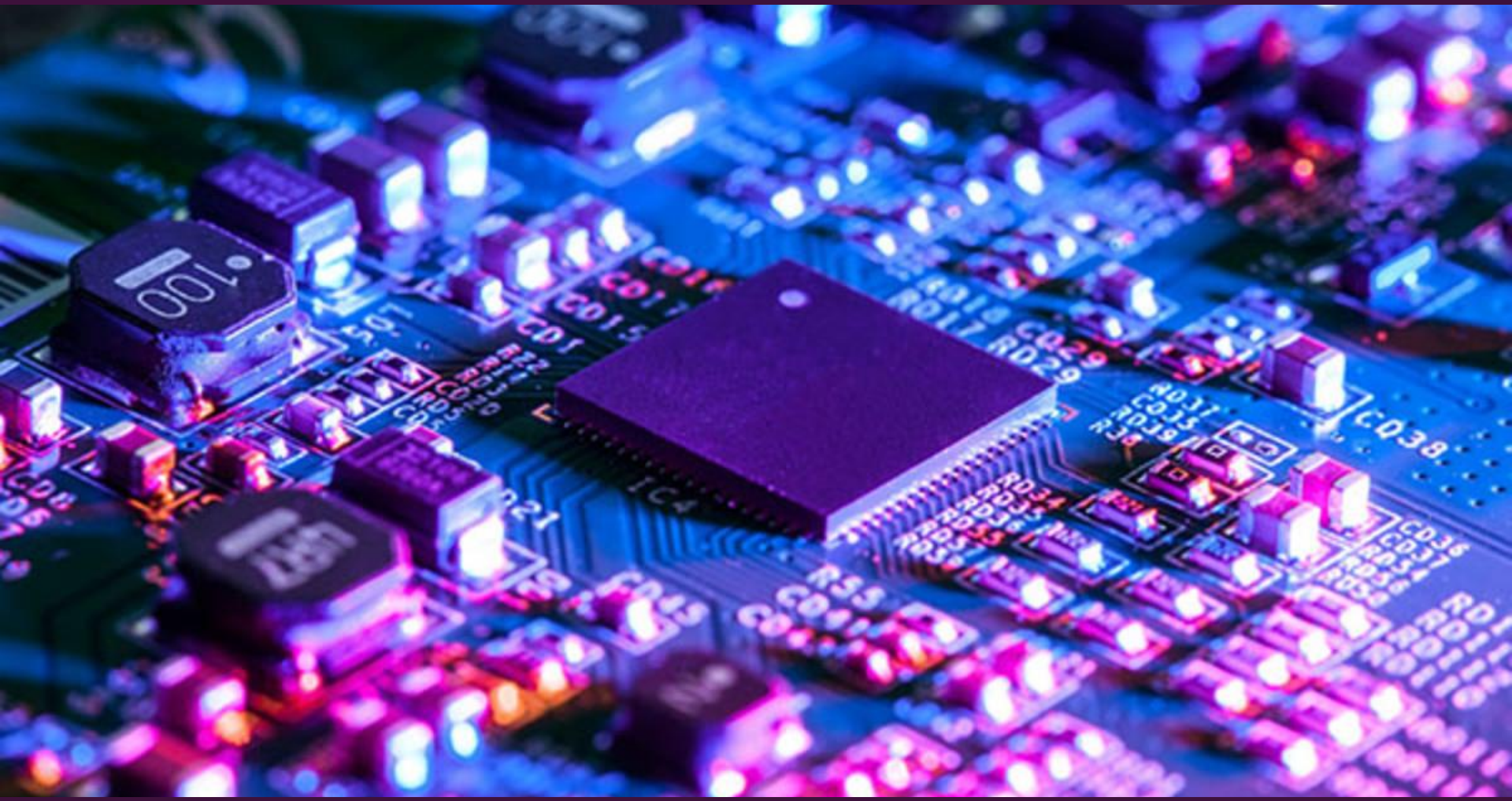
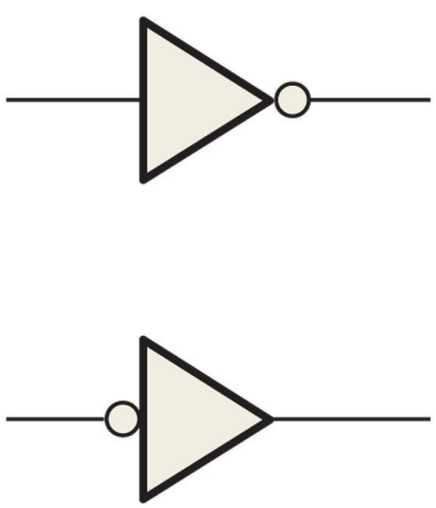
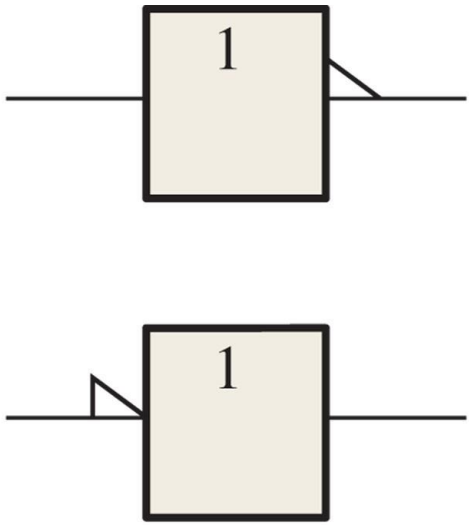


FIGURE 3-1 Standard logic symbols for the inverter (ANSI/IEEE Std. 91-1984/Std. 91a-1991).



(a) Distinctive shape symbols with negation indicators



(b) Rectangular outline symbols with polarity indicators

TABLE 3–1

Inverter truth table.

Input	Output
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)

FIGURE 3-2 Inverter operation with a pulse input.

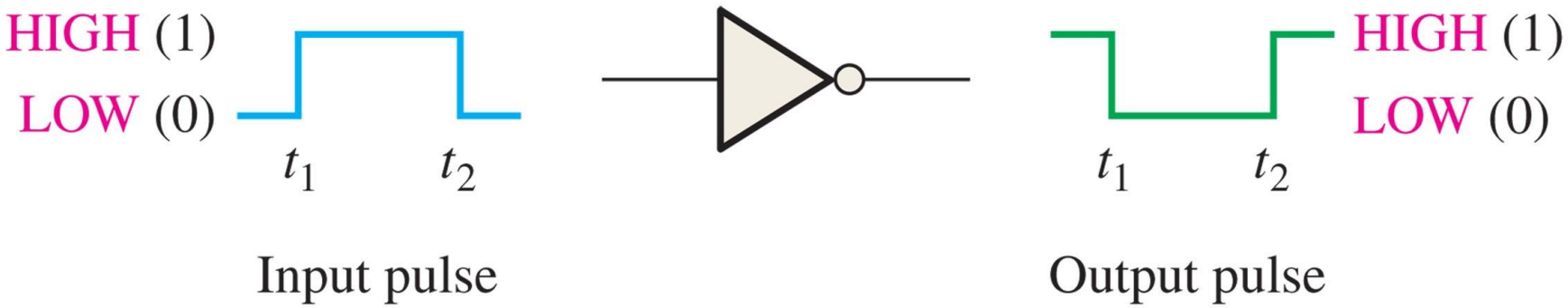


FIGURE 3-6 The inverter complements an input variable.

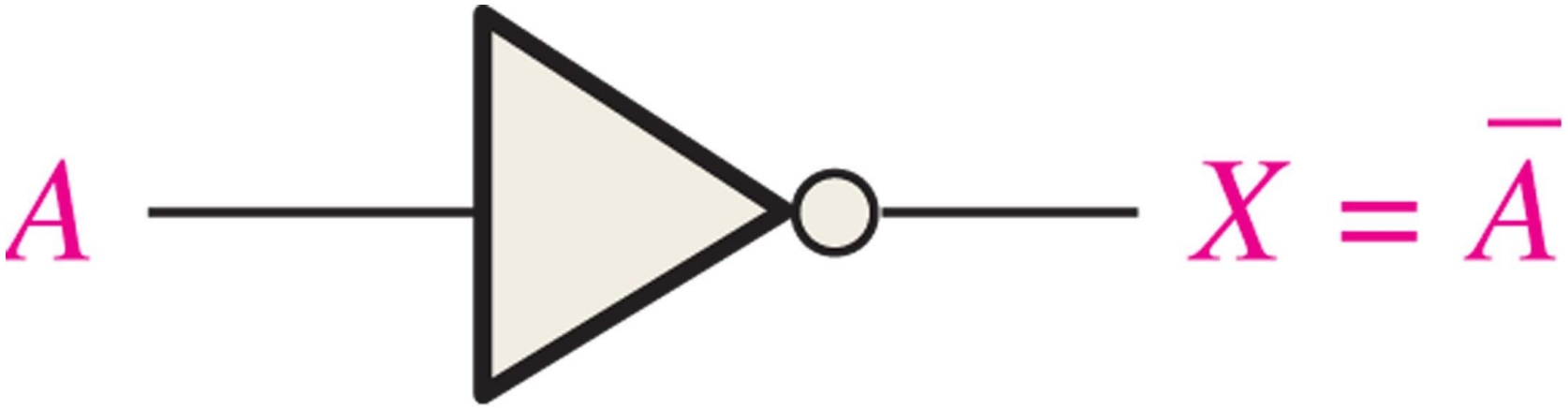


FIGURE 3-7 Example of a 1's complement circuit using inverters.

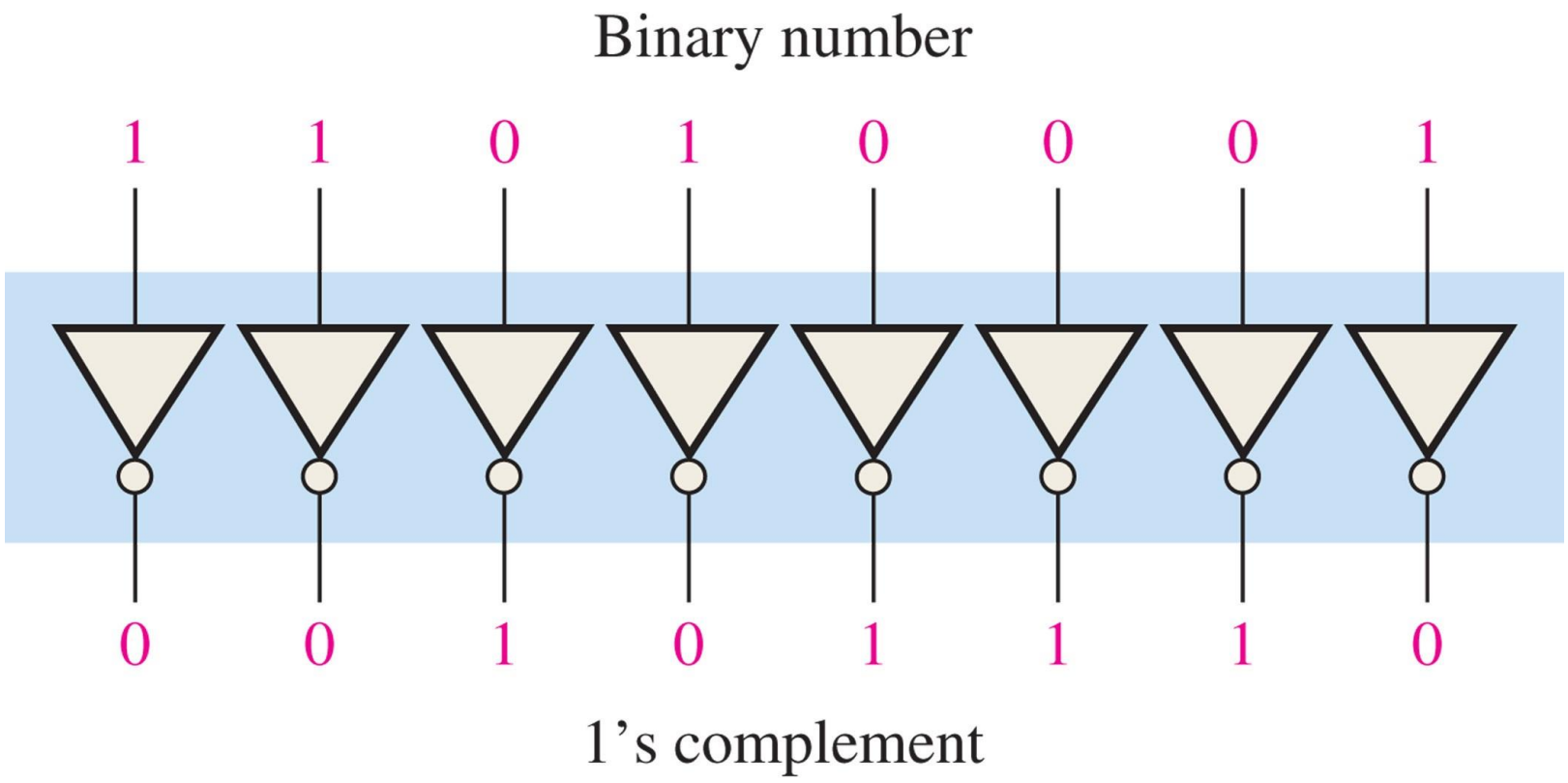


FIGURE 3-8 Standard logic symbols for the AND gate showing two inputs (ANSI/IEEE Std. 91-1984/Std. 91a-1991).

(a) Distinctive shape

(b) Rectangular outline with the AND (&) qualifying symbol

FIGURE 3-9 All possible logic levels for a 2-input AND gate.

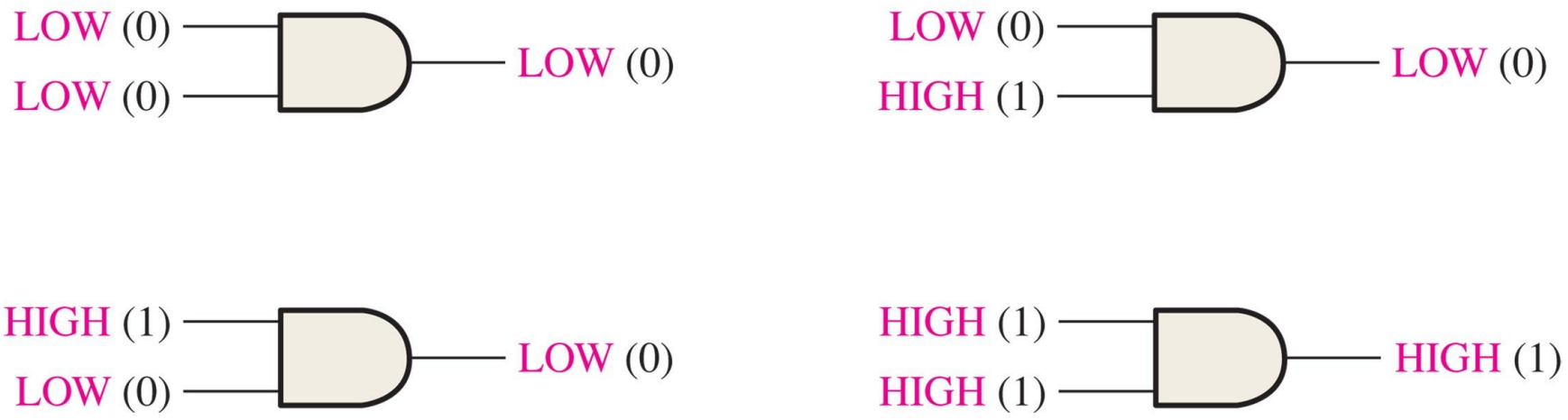


TABLE 3–2

Truth table for a 2-input AND gate.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	0
1	0	0
1	1	1

1 = HIGH, 0 = LOW

TABLE 3–3

Inputs			Output
A	*B*	*C*	*X*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

FIGURE 3-10 Example of AND gate operation with a timing diagram showing input and output relationships.

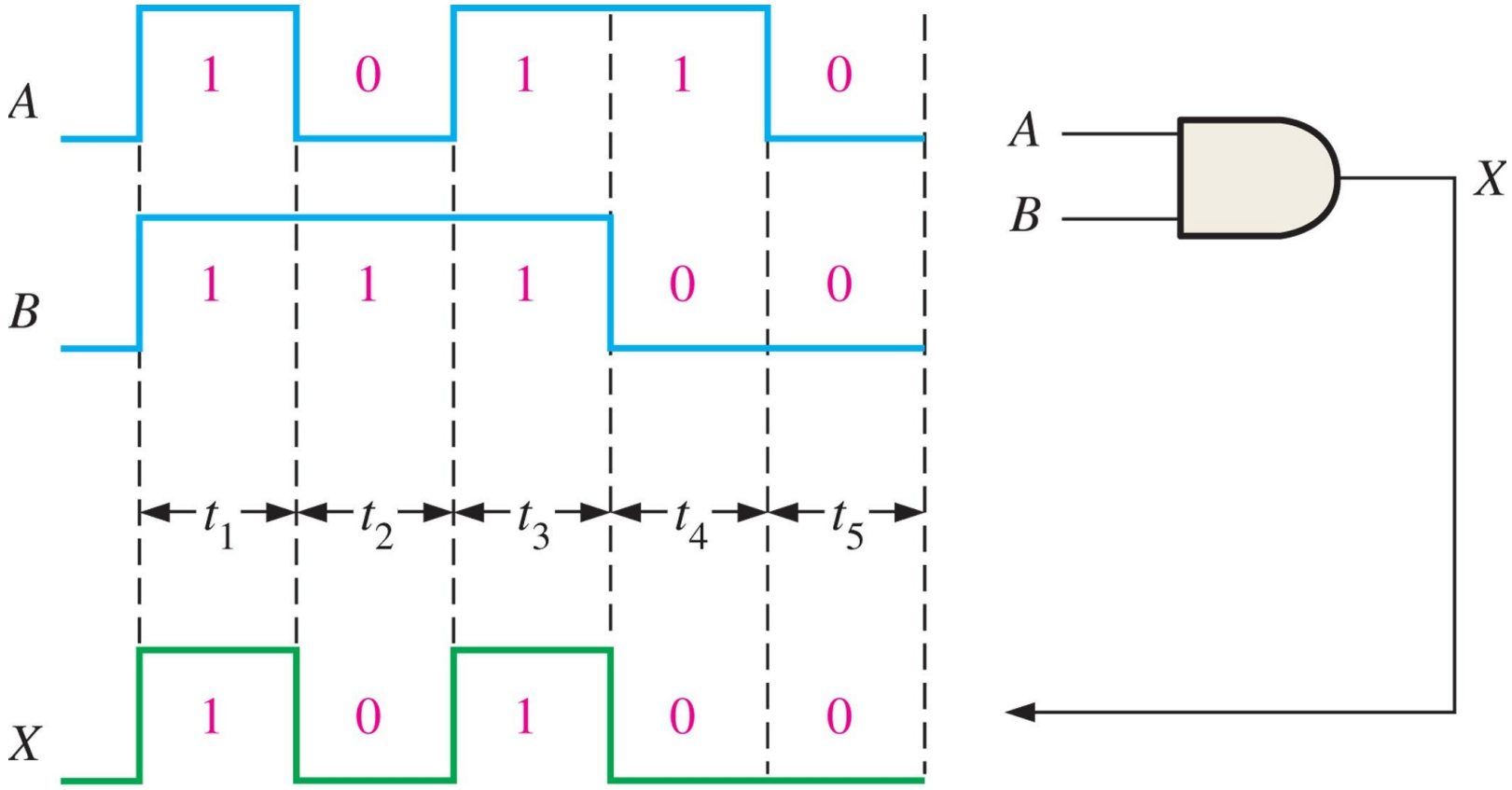


FIGURE 3-15 Boolean expressions for AND gates with two, three, and four inputs.

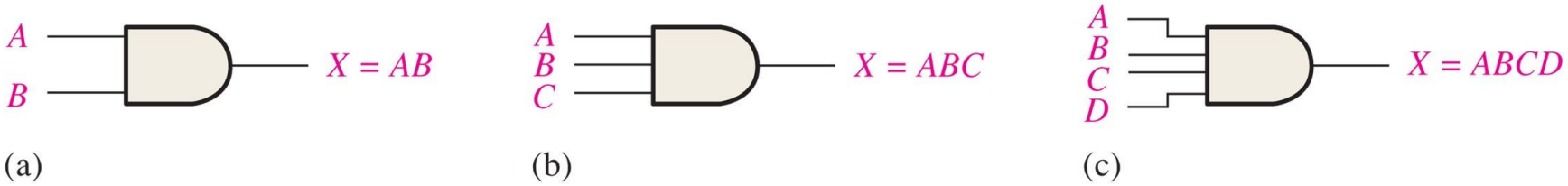


FIGURE 3-16 An AND gate performing an enable/inhibit function for a frequency counter.

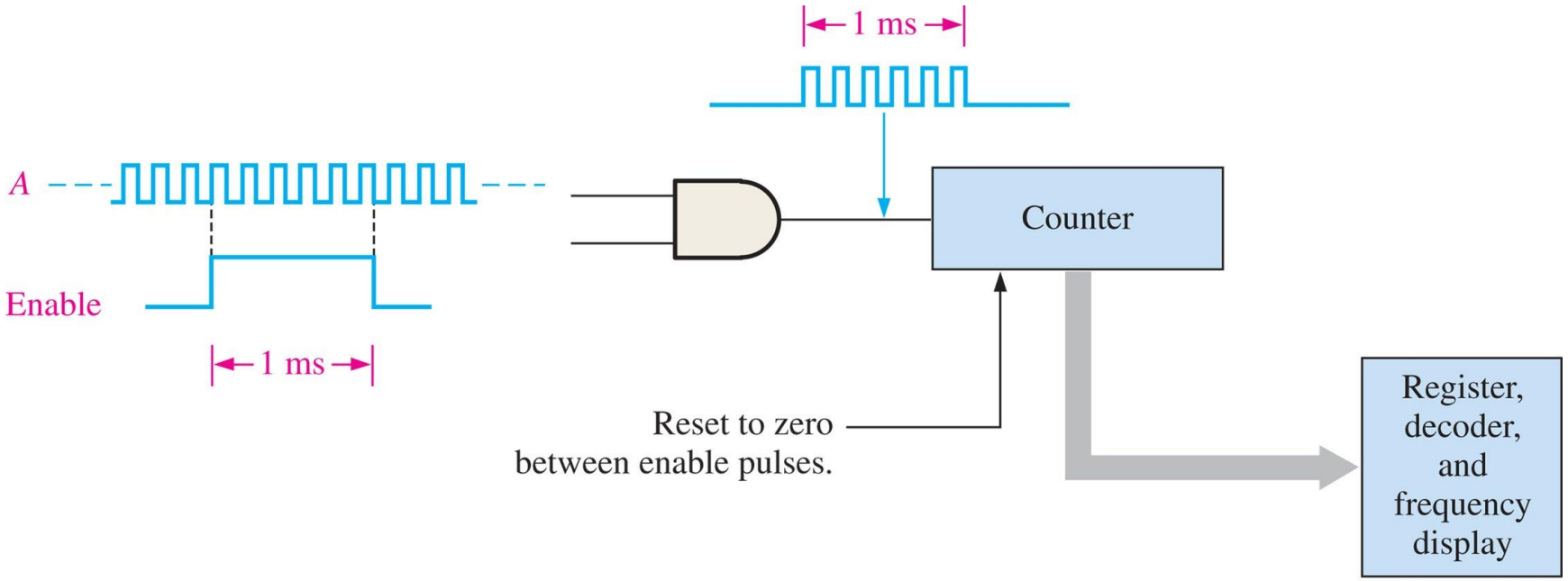


FIGURE 3-17 A simple seat belt alarm circuit using an AND gate.

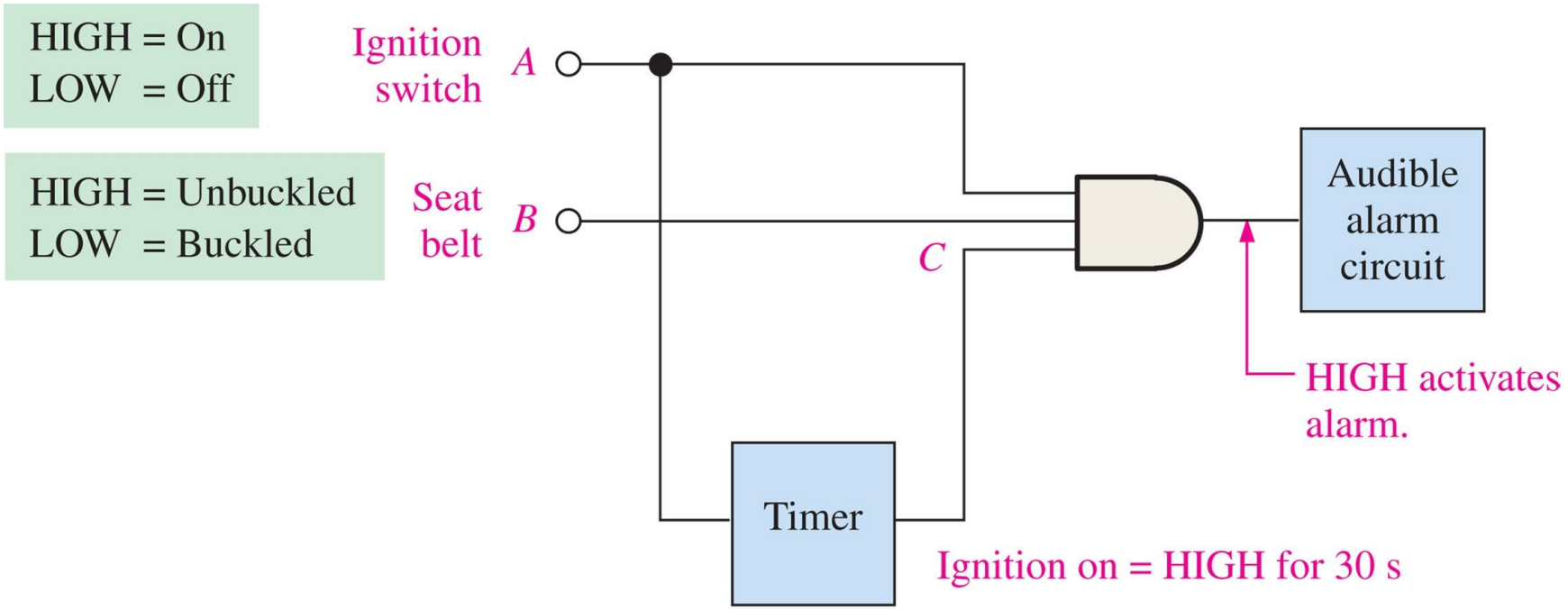
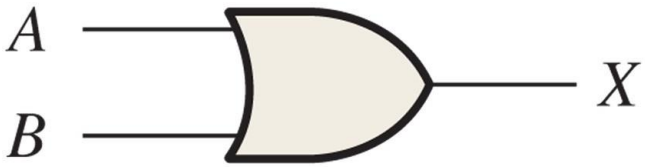
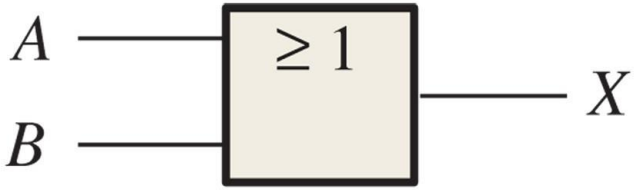


FIGURE 3-18 Standard logic symbols for the OR gate showing two inputs (ANSI/IEEE Std. 91-1984/Std. 91a-1991).



(a) Distinctive shape



(b) Rectangular outline with the OR (≥ 1) qualifying symbol

FIGURE 3-19 All possible logic levels for a 2-input OR gate.

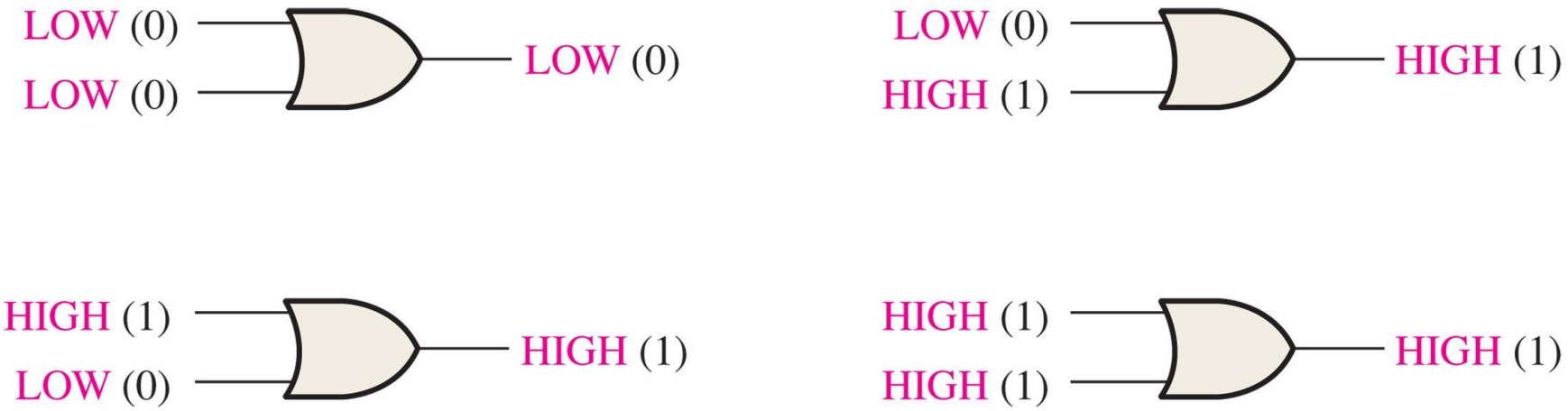


TABLE 3–5

Truth table for a 2-input OR gate.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	1

1 = HIGH, 0 = LOW

FIGURE 3-20 Example of OR gate operation with a timing diagram showing input and output time elationships.

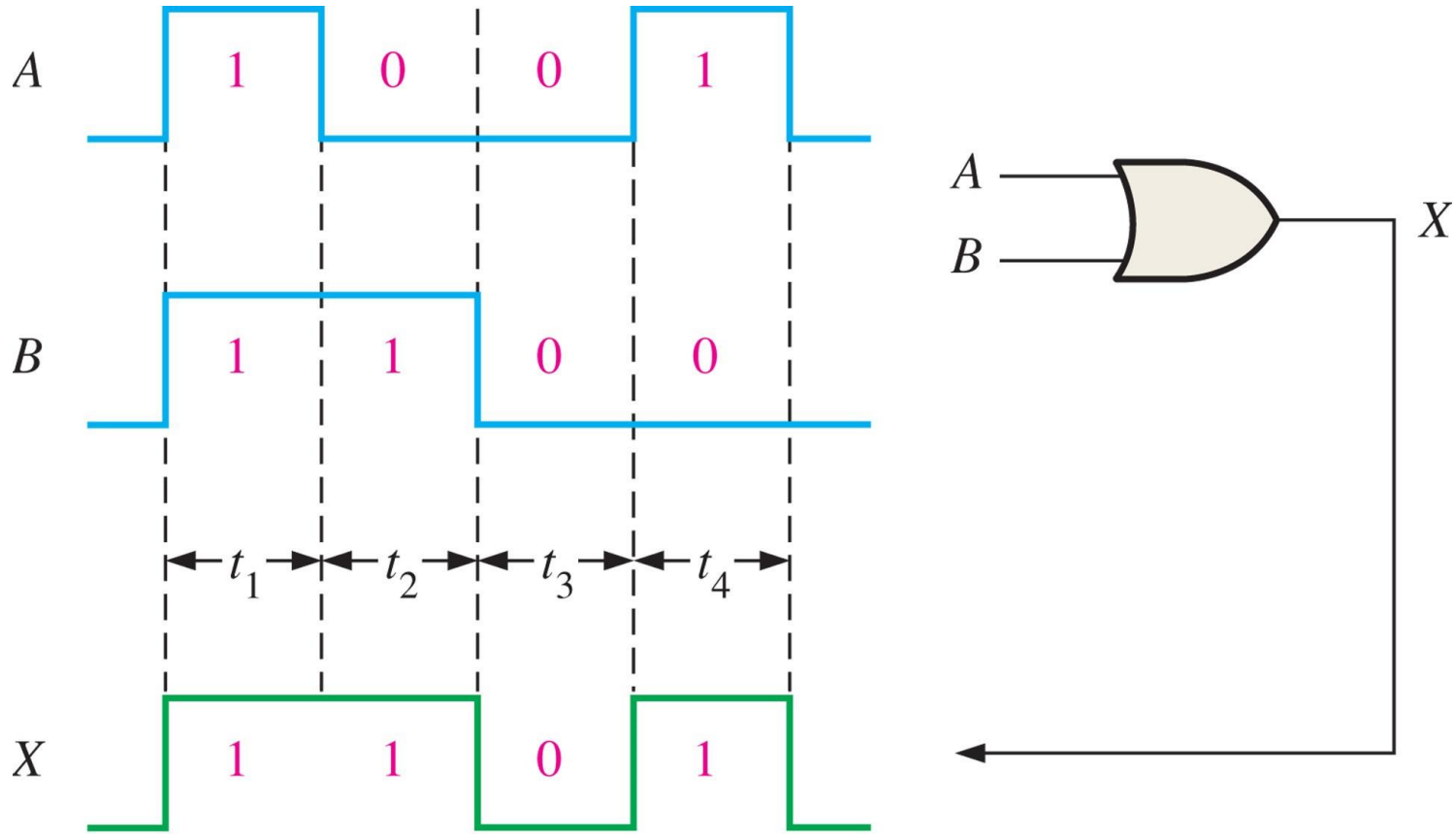


FIGURE 3-24 Boolean expressions for OR gates with two, three, and four inputs.

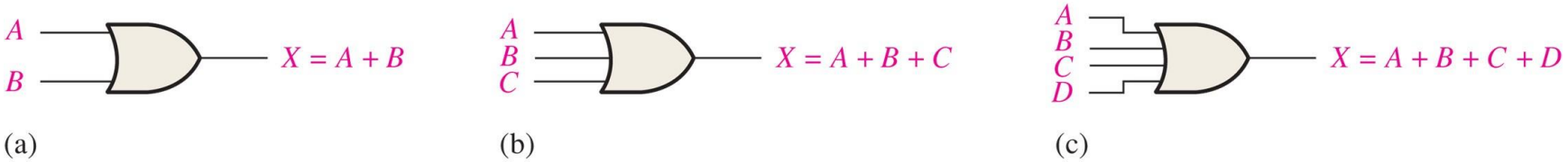


FIGURE 3-25 A simplified intrusion detection system using an OR gate.

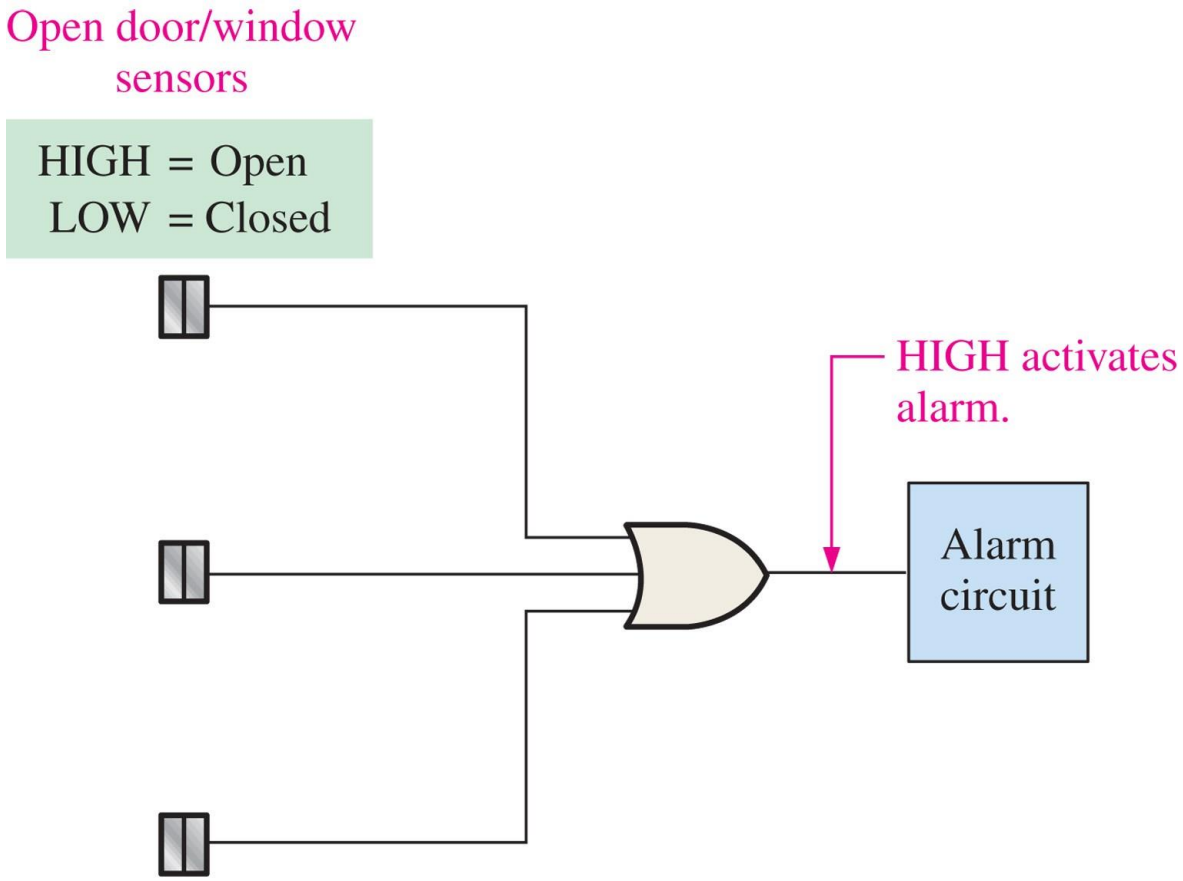
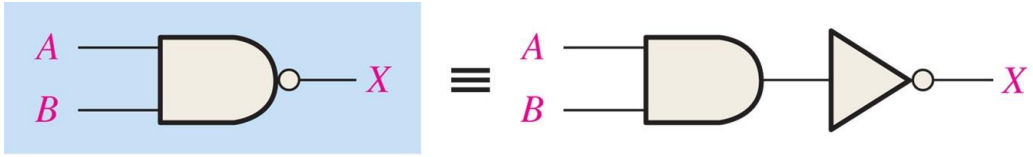
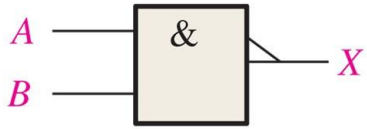


FIGURE 3-26 Standard NAND gate logic symbols (ANSI/IEEE Std. 91-1984/Std. 91a-1991).



(a) Distinctive shape, 2-input NAND gate and its NOT/AND equivalent



(b) Rectangular outline, 2-input NAND gate with polarity indicator

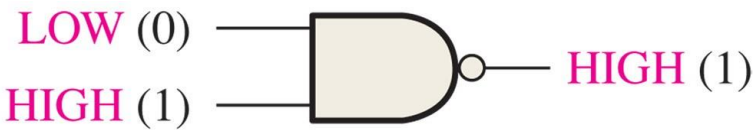
TABLE 3–7

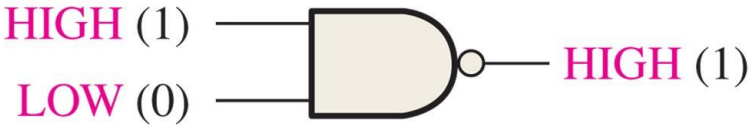
Truth table for a 2-input NAND gate.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	1
1	0	1
1	1	0

1 = HIGH, 0 = LOW.

FIGURE 3-27 Operation of a 2-input NAND gate.





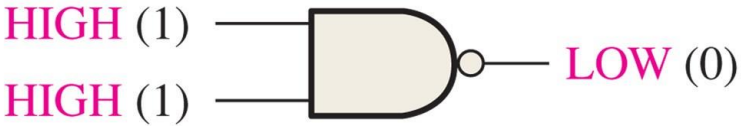
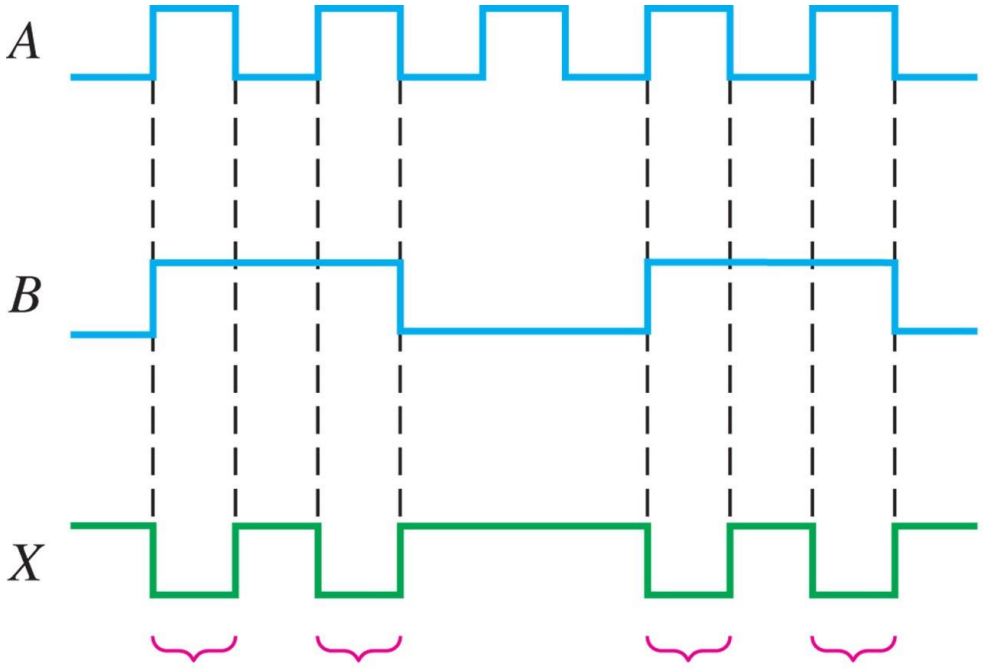


FIGURE 3-28



A and *B* are both HIGH during these four time intervals; therefore, *X* is LOW.

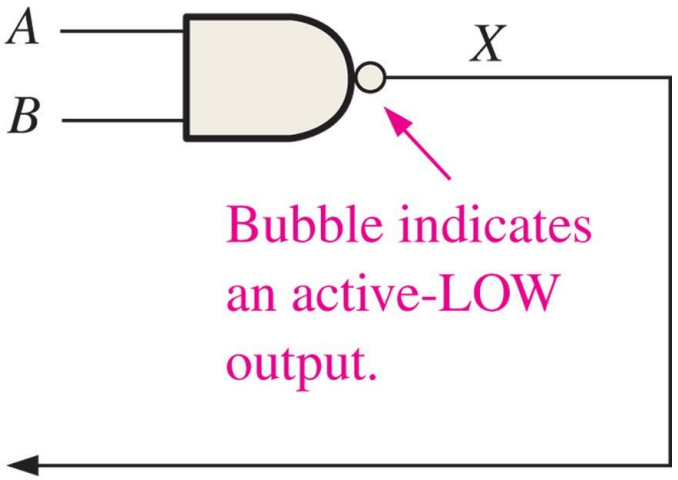


FIGURE 3-29

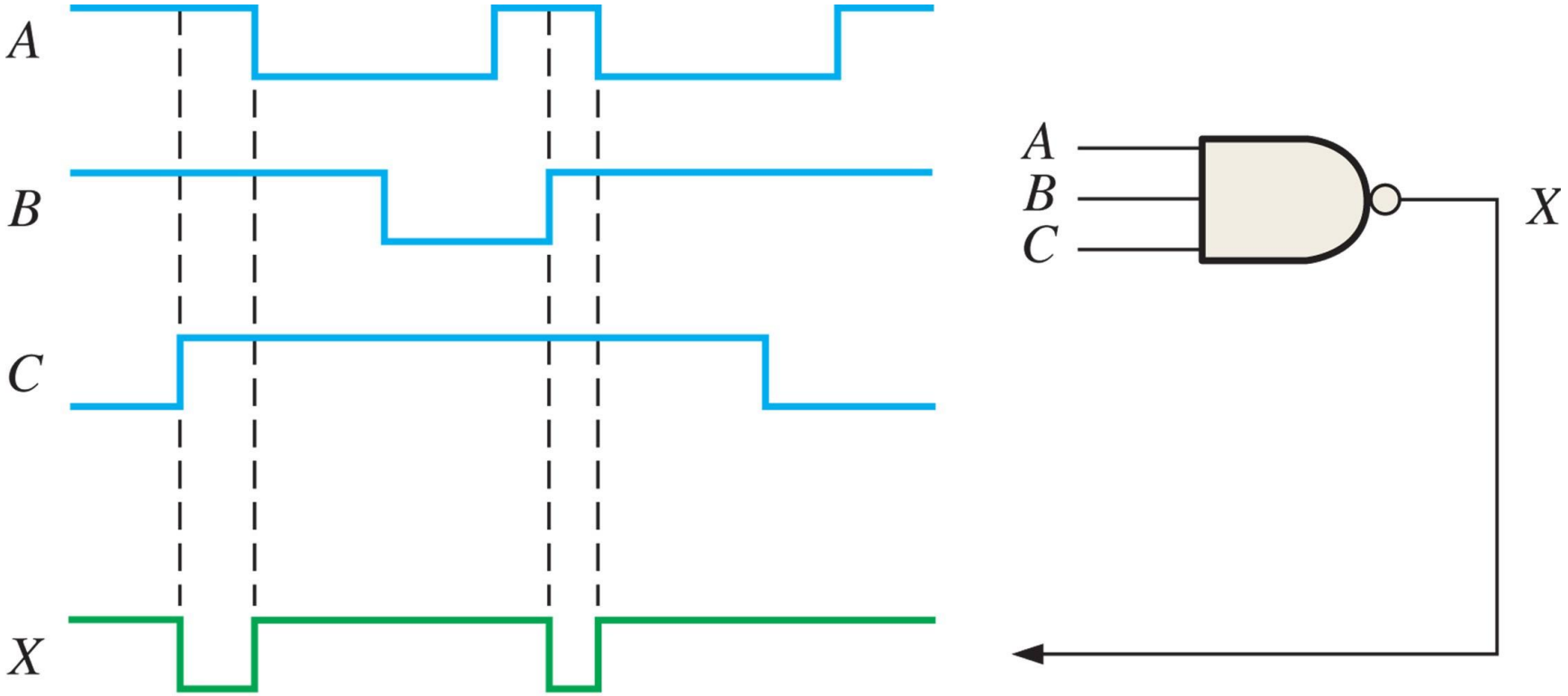


FIGURE 3-30 ANSI/IEEE standard symbols representing the two equivalent operations of a NAND gate.

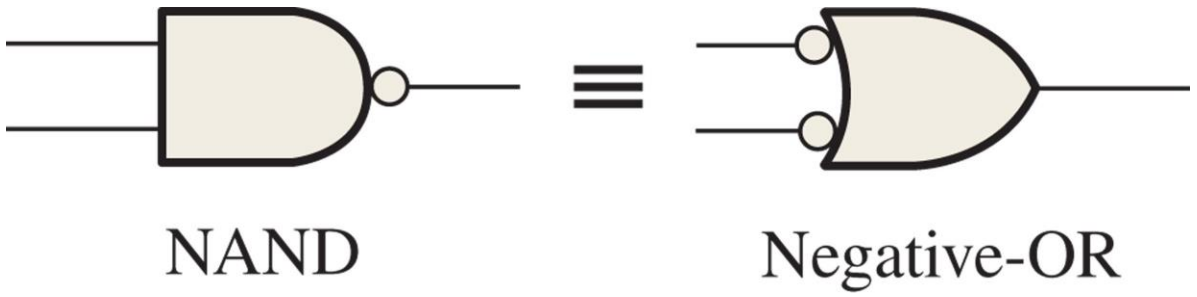


FIGURE 3-31

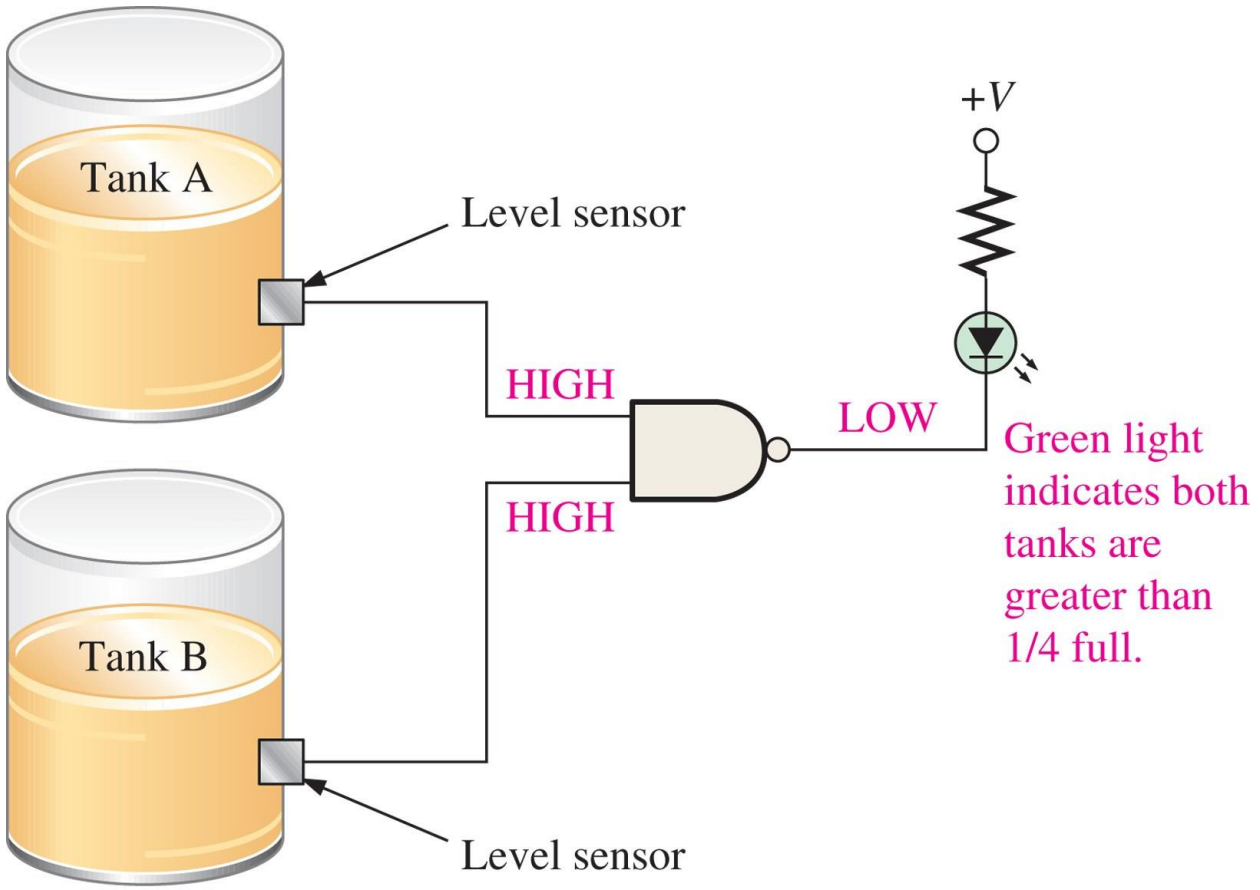

Tank A
Level sensor
+V
HIGH
LOW
Green light indicates both tanks are greater than 1/4 full.
HIGH
Tank B
Level sensor

FIGURE 3-32

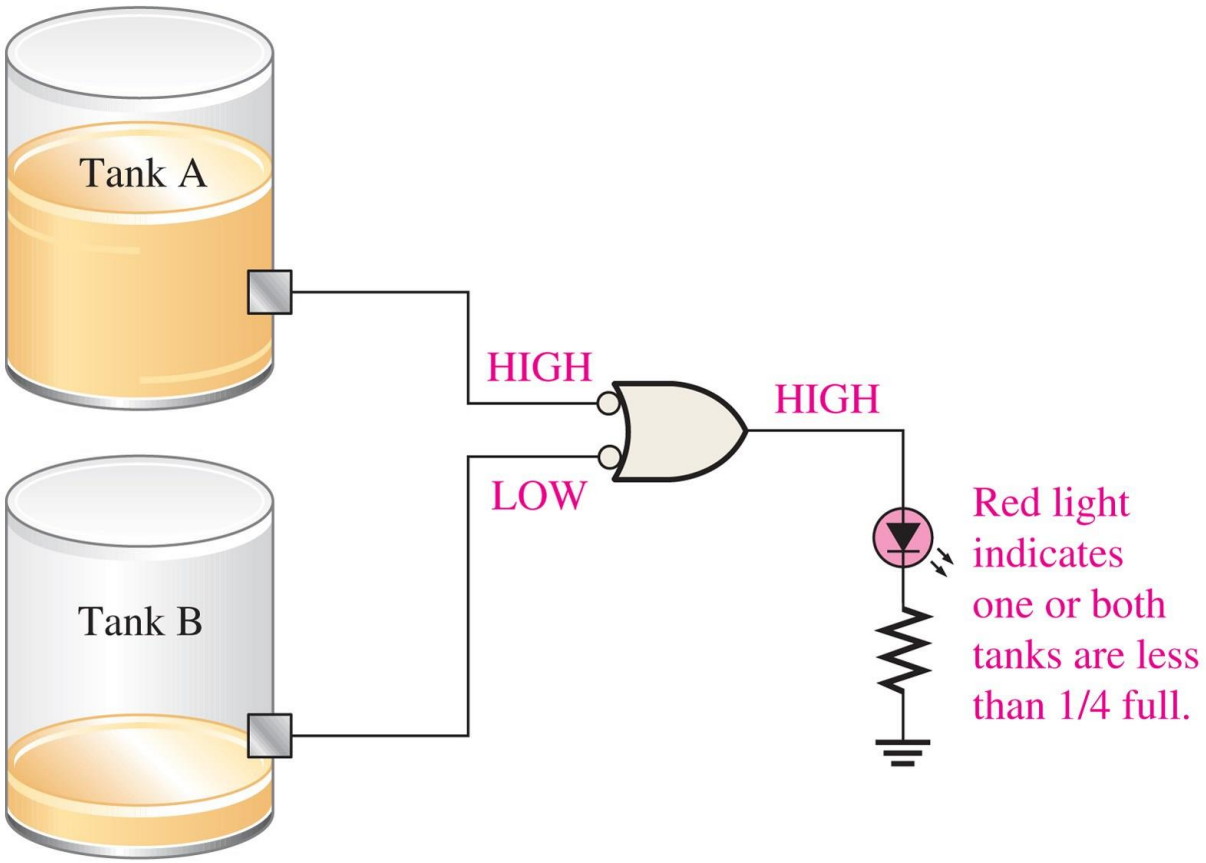

Tank A
Tank B
HIGH
LOW
HIGH
Red light indicates one or both tanks are less than 1/4 full.

FIGURE 3-33

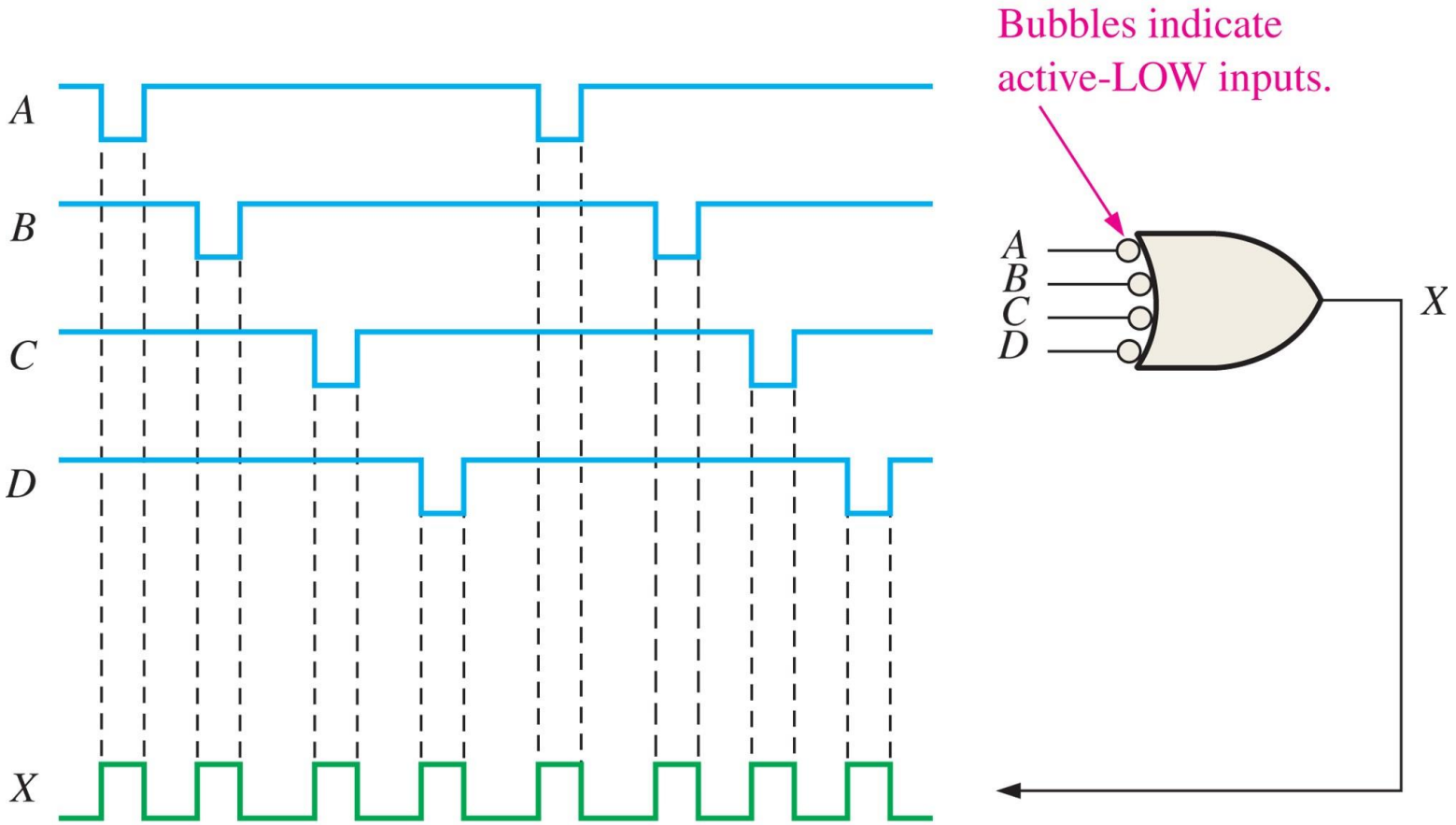
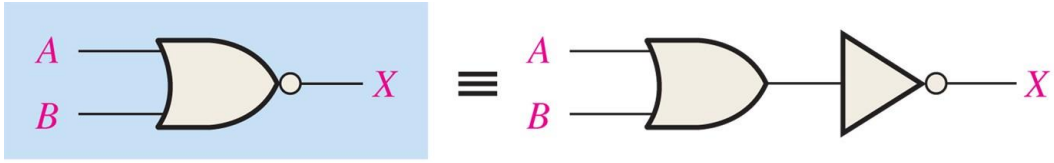
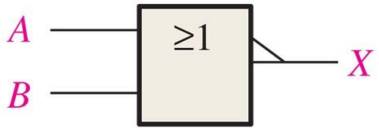


FIGURE 3-34 Standard NOR gate logic symbols (ANSI/IEEE Std. 91-1984/Std. 91a-1991).



(a) Distinctive shape, 2-input NOR gate and its NOT/OR equivalent



(b) Rectangular outline, 2-input NOR gate with polarity indicator

FIGURE 3-35 Operation of a 2-input NOR gate.

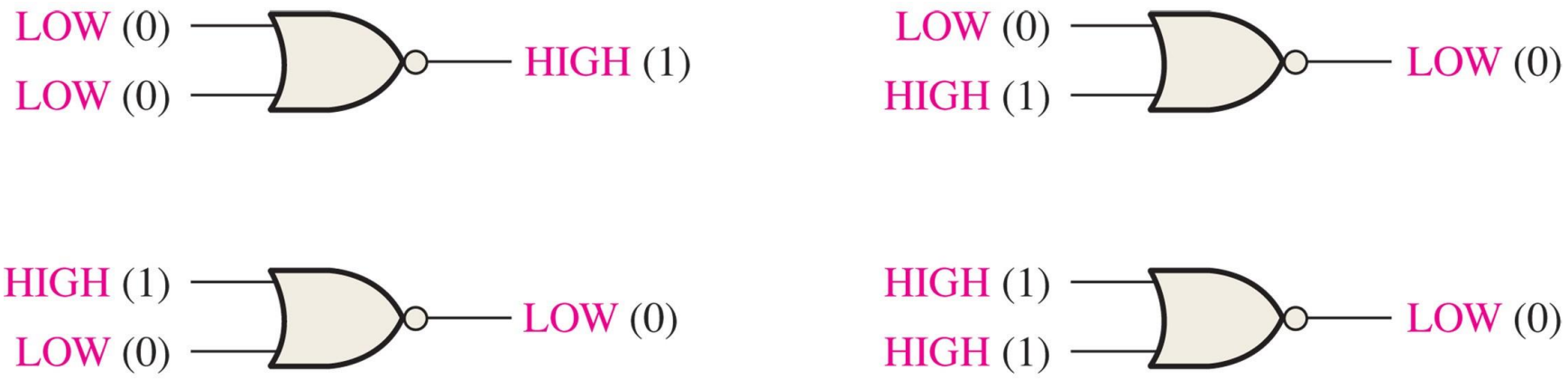


TABLE 3–9

Truth table for a 2-input NOR gate.

Inputs		Output
A	***B***	***X***
0	0	1
0	1	0
1	0	0
1	1	0

1 = HIGH, 0 = LOW.

FIGURE 3-36

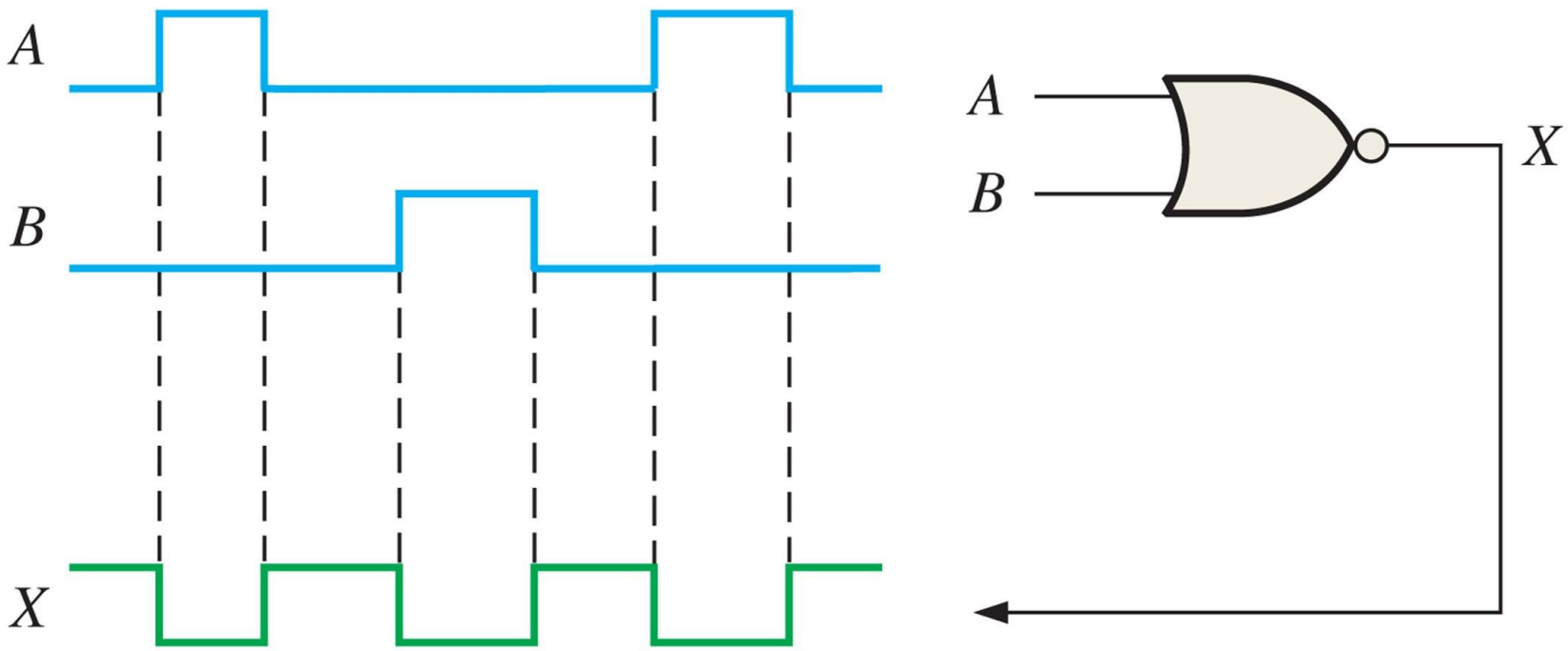


FIGURE 3-37

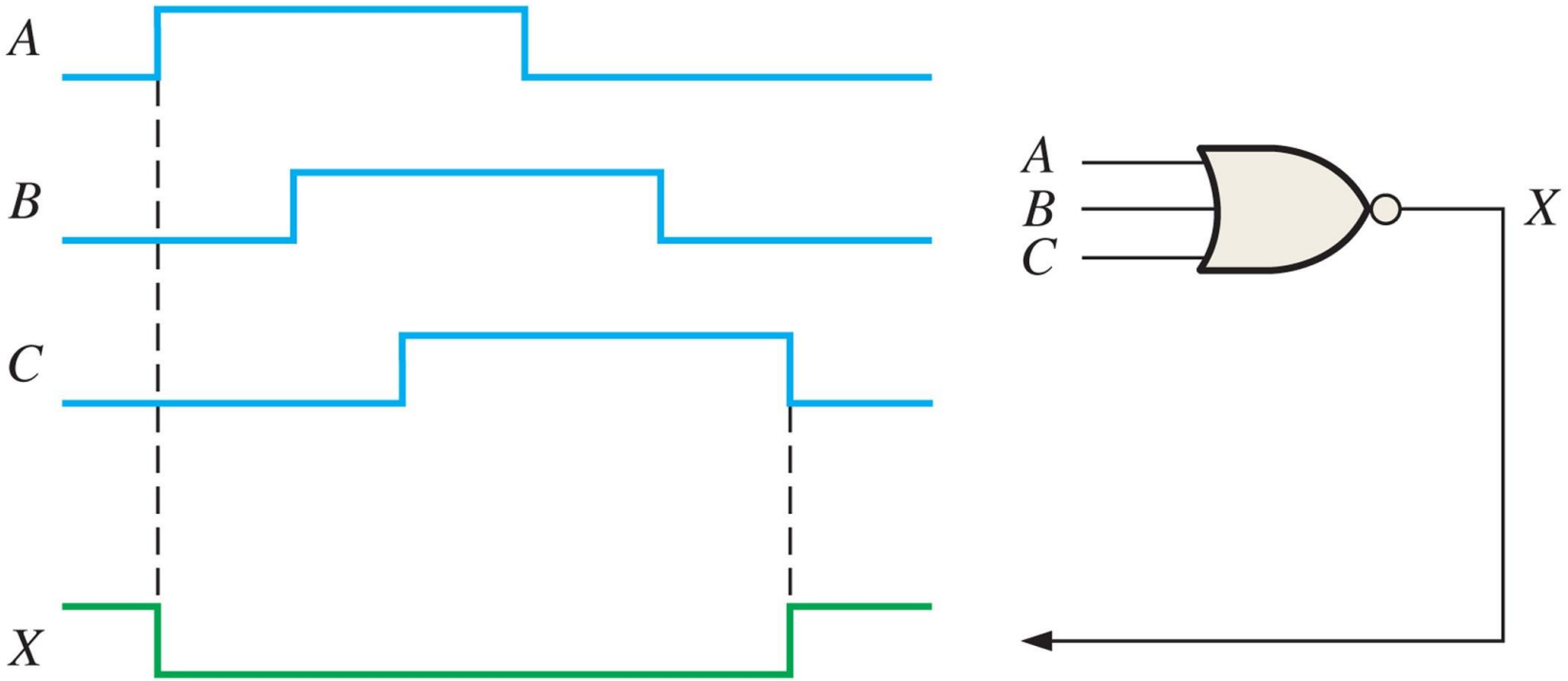


FIGURE 3-38 Standard symbols representing the two equivalent operations of a NOR gate.

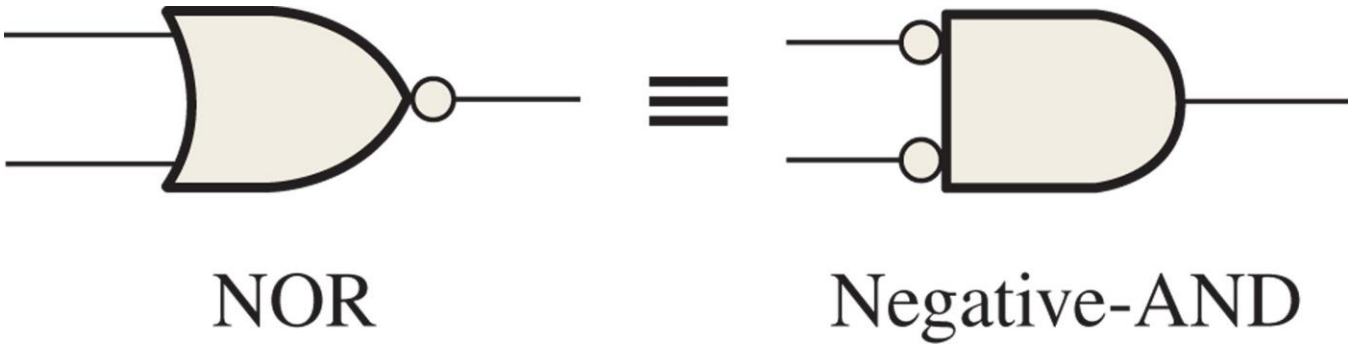


FIGURE 3-40

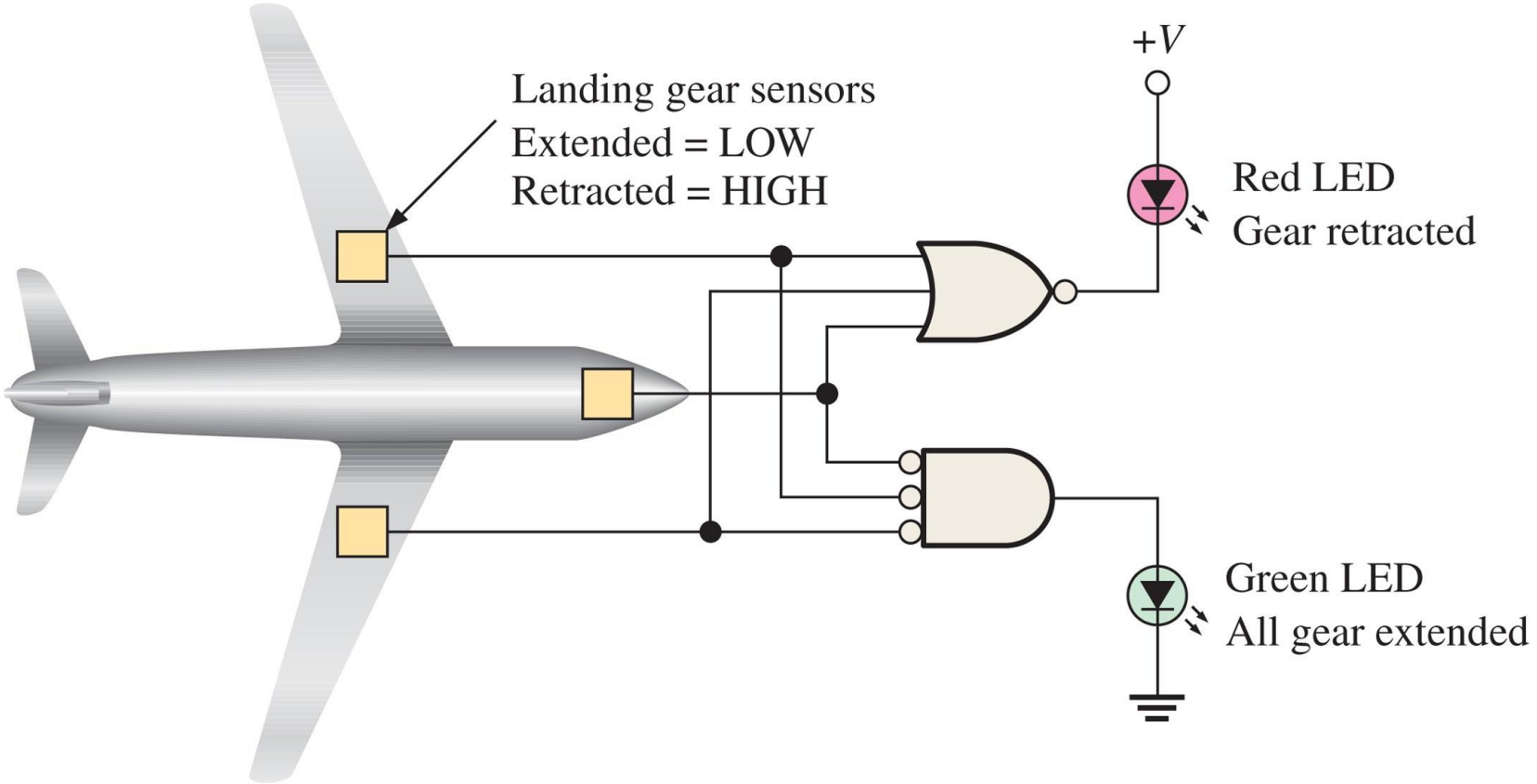

Landing gear sensors
Extended = LOW
Retracted = HIGH
+V
Red LED
Gear retracted
Green LED
All gear extended

FIGURE 3-41

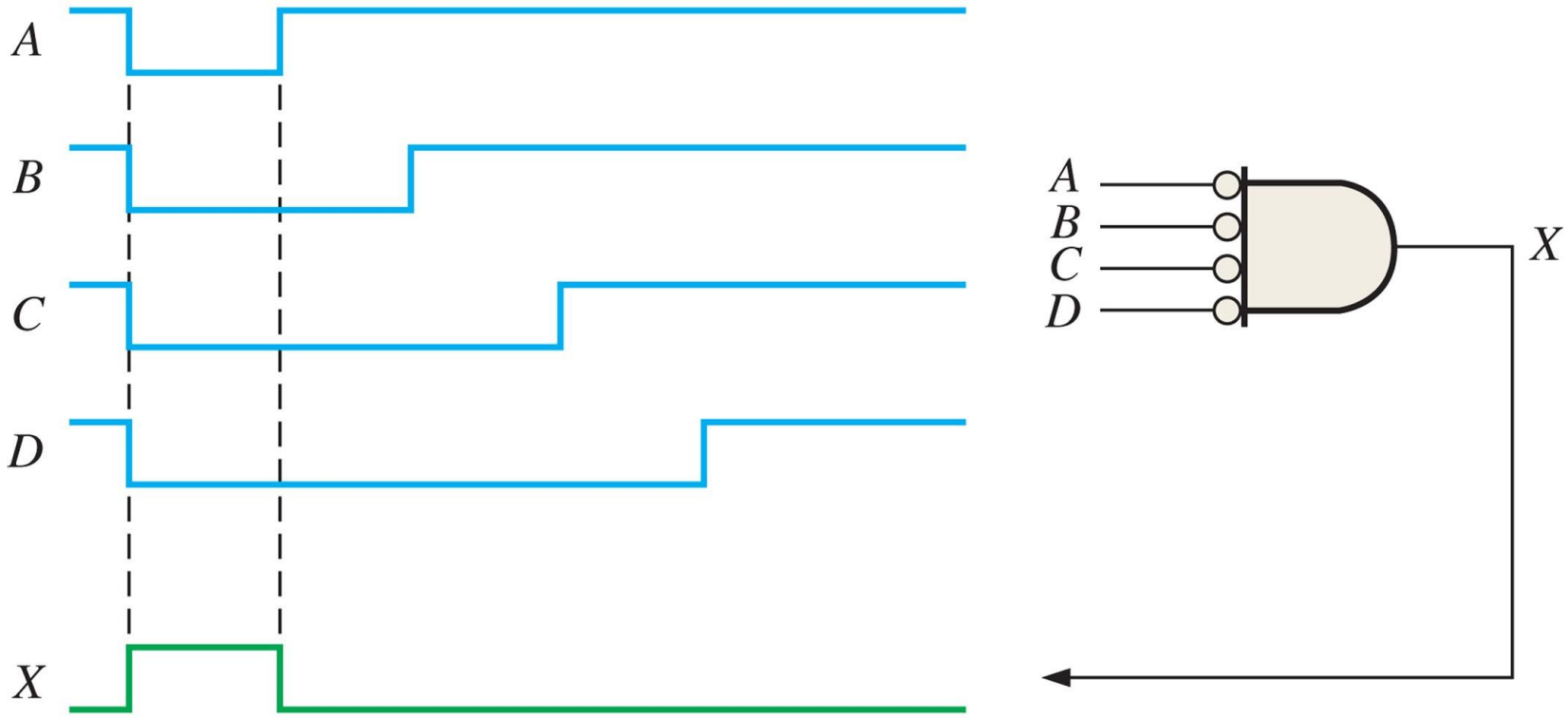
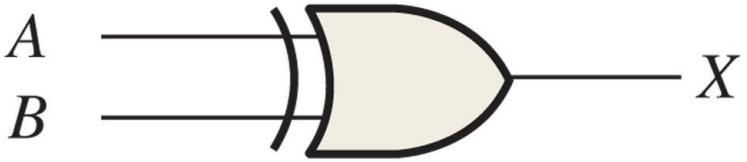
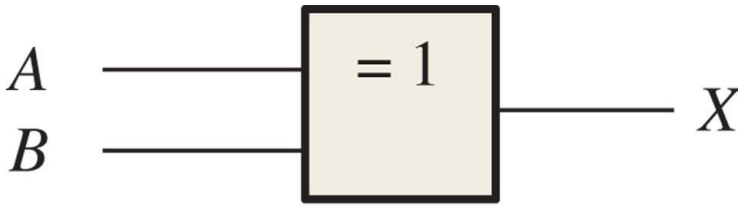


FIGURE 3-42 Standard logic symbols for the exclusive-OR gate.



(a) Distinctive shape



(b) Rectangular outline

TABLE 3–11

Truth table for an exclusive-OR gate.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	0

FIGURE 3-43 All possible logic levels for an exclusive-OR gate.

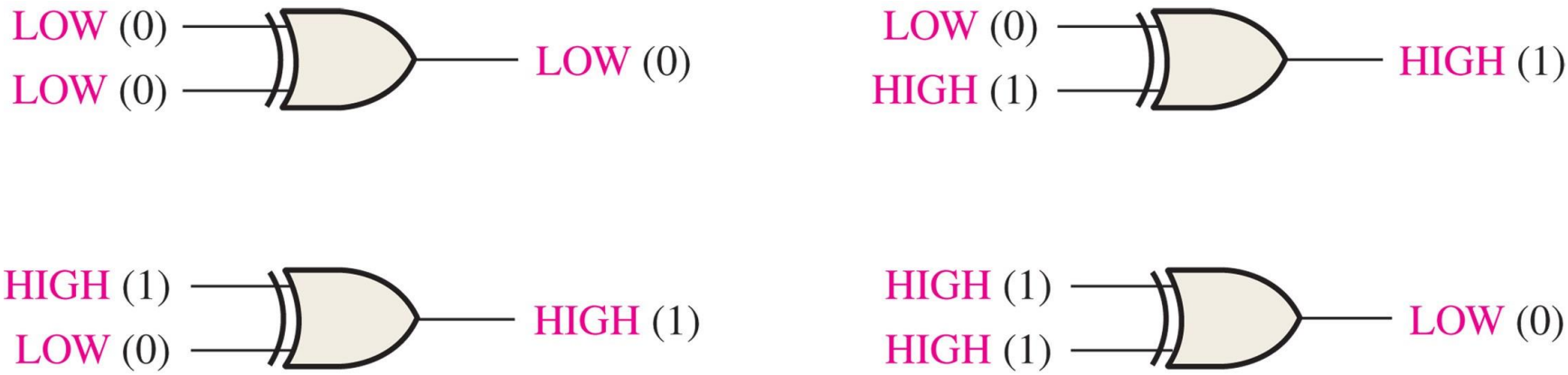
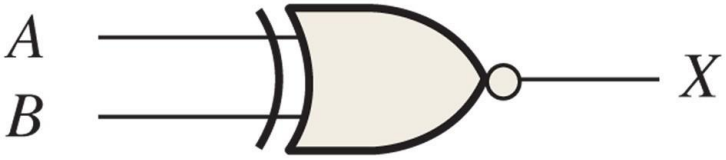
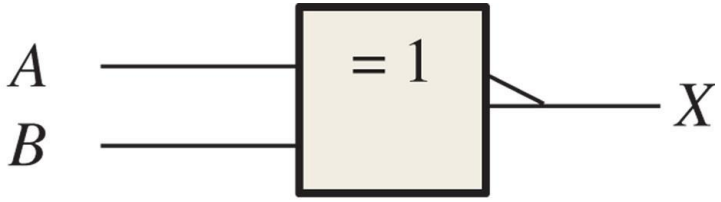


FIGURE 3-45 Standard logic symbols for the exclusive-NOR gate.



(a) Distinctive shape



(b) Rectangular outline

TABLE 3–12

Truth table for an exclusive-NOR gate.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	1

FIGURE 3-46 All possible logic levels for an exclusive-NOR gate.

FIGURE 3-47 Example of exclusive-OR gate operation with pulse waveform inputs.

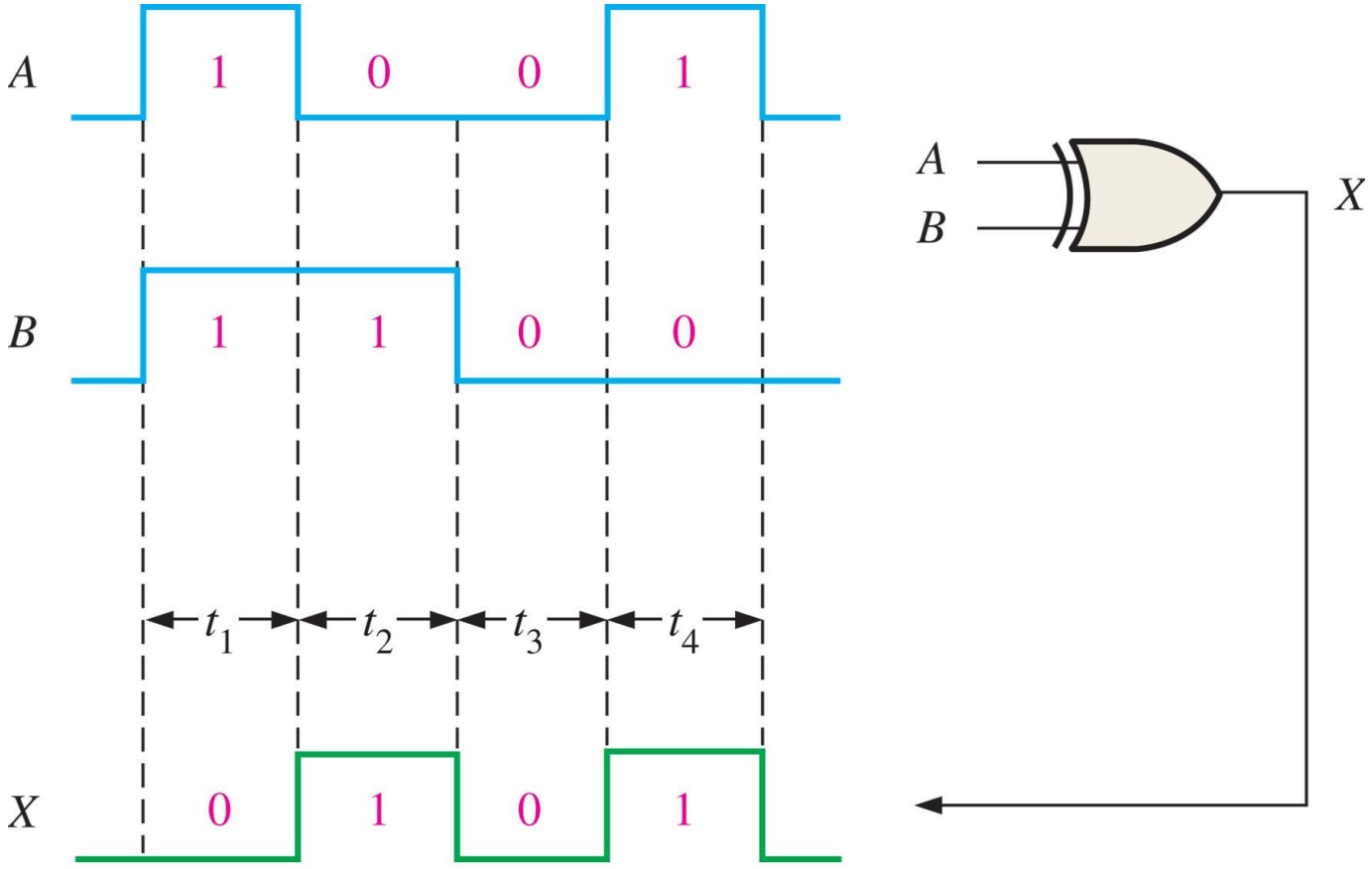


FIGURE 3-48

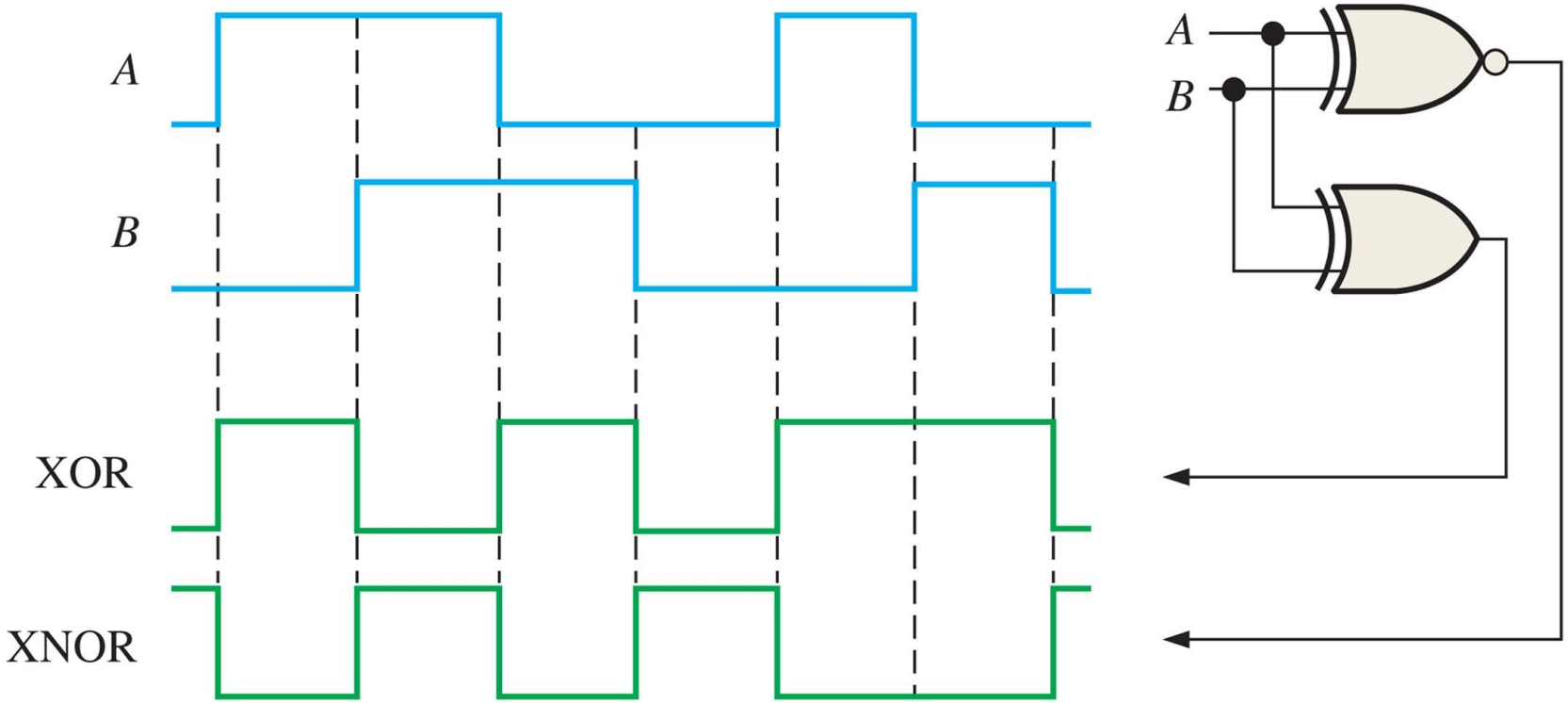


TABLE 3–13

An XOR gate used to add two bits.

Input Bits		Output (Sum)	
A	*B*	Σ	
0	0	0	
0	1	1	
1	0	1	
1	1	0	(without the 1 carry bit)

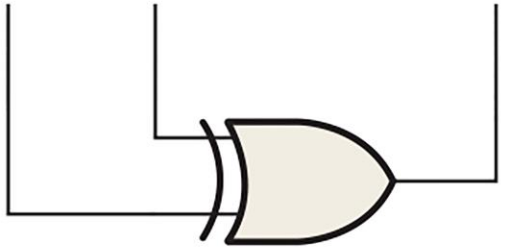
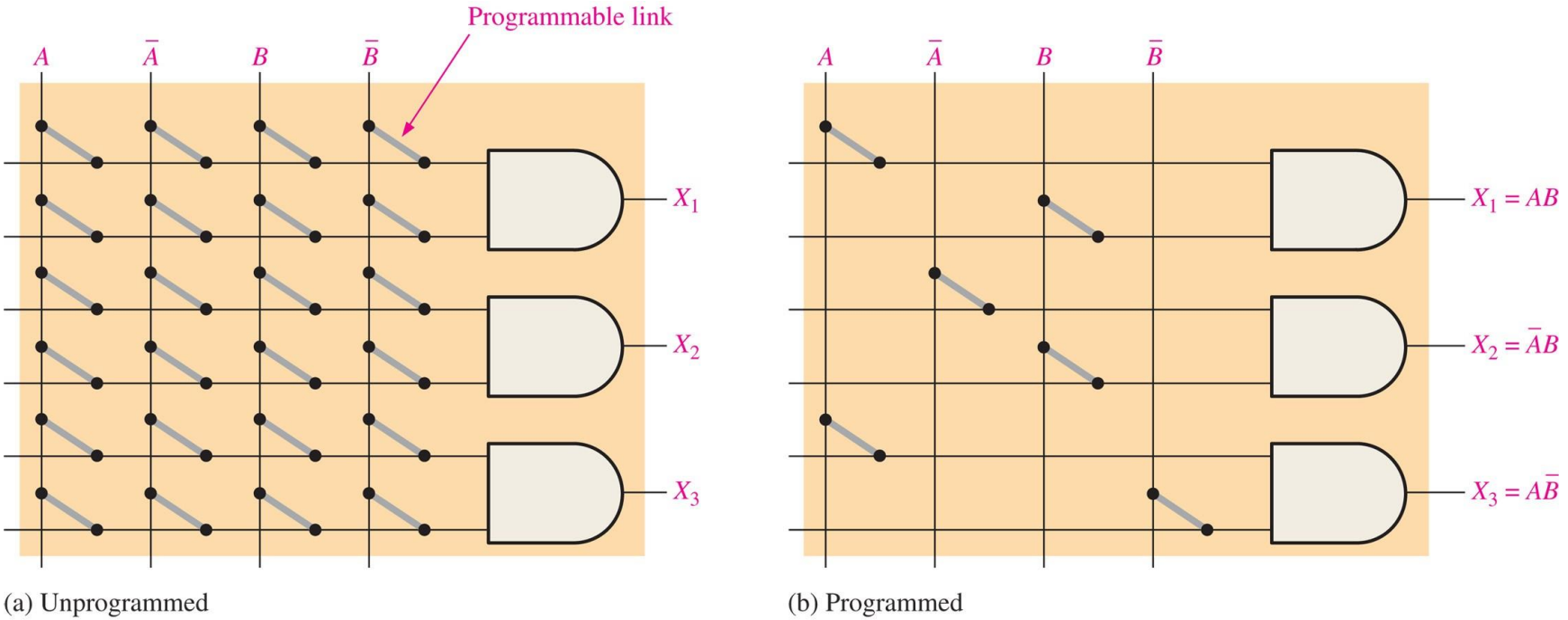


FIGURE 3-49 Concept of a programmable AND array.



(a) Unprogrammed

(b) Programmed

FIGURE 3-50

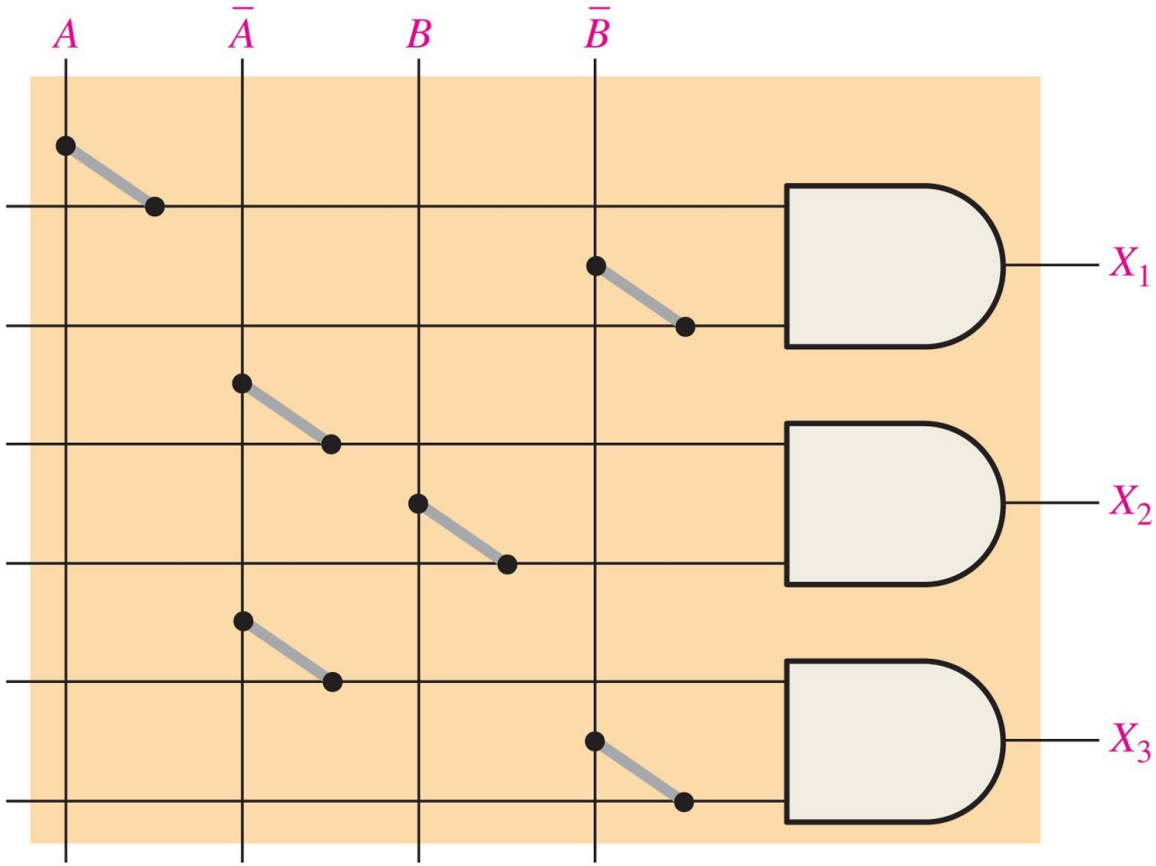
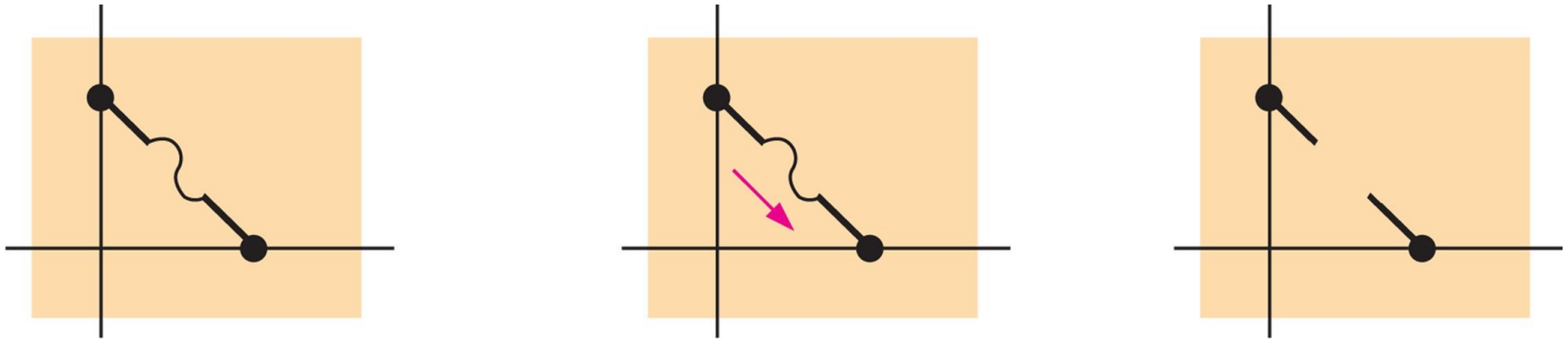


FIGURE 3-51 The programmable fuse link.

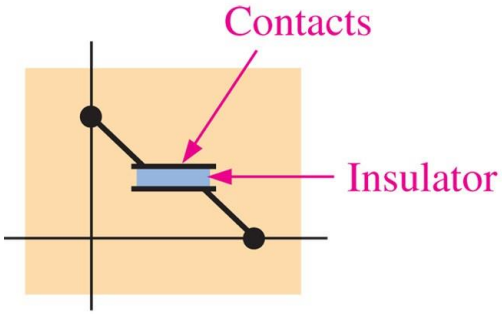


(a) Fuse intact before programming

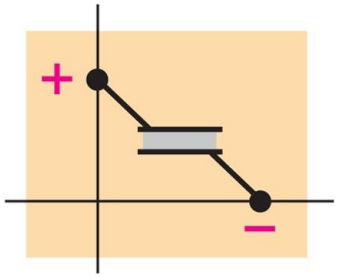
(b) Programming current

(c) Fuse open after programming

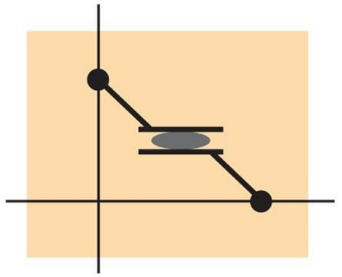
FIGURE 3-52 The programmable antifuse link.



(a) Antifuse is open before programming.



(b) Programming voltage breaks down insulation layer to create contact.



(c) Antifuse is effectively shorted after programming.

FIGURE 3-53 A simple AND array with EPROM technology. Only one gate in the array is shown for simplicity.

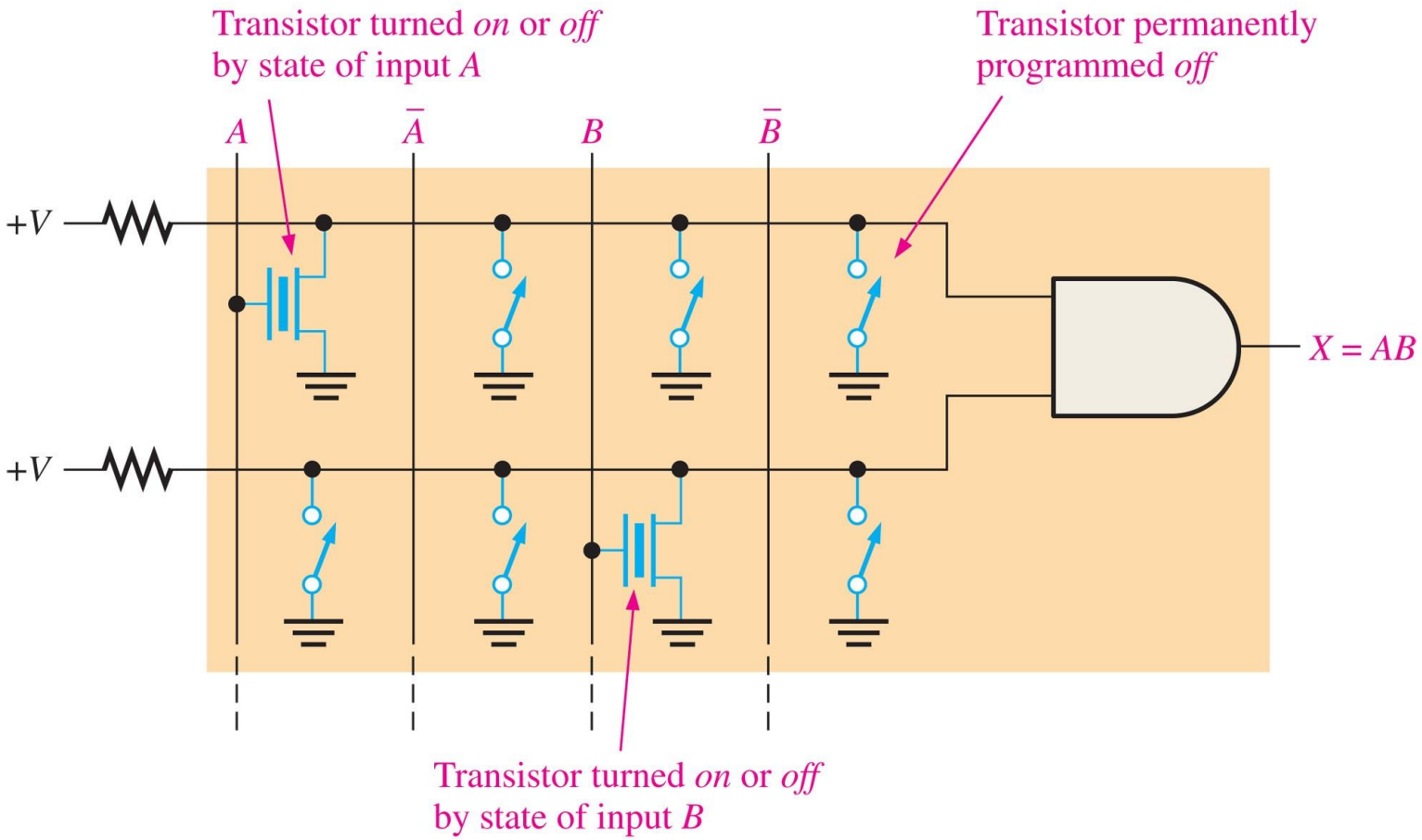
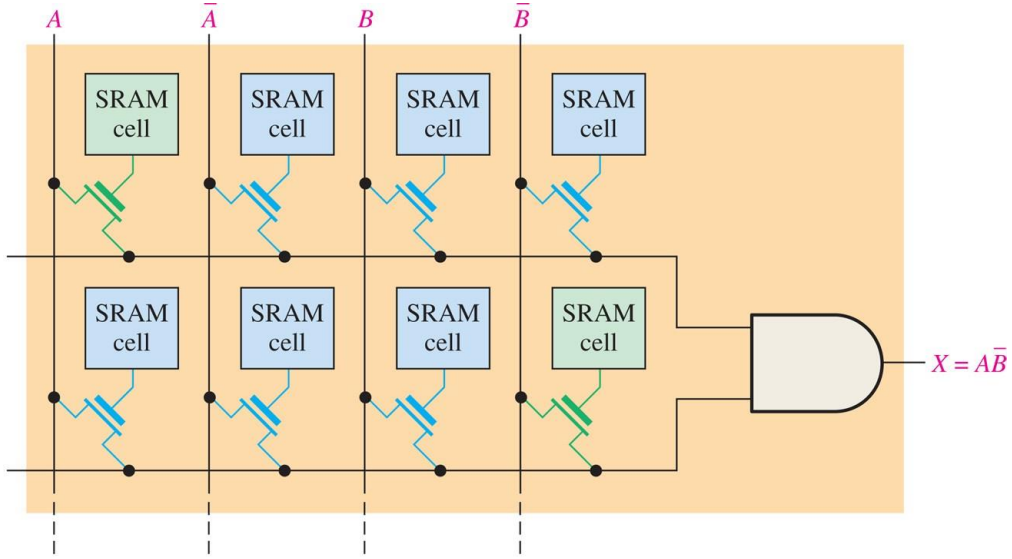
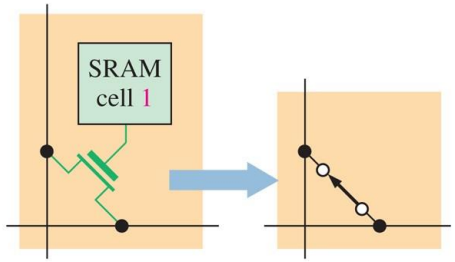


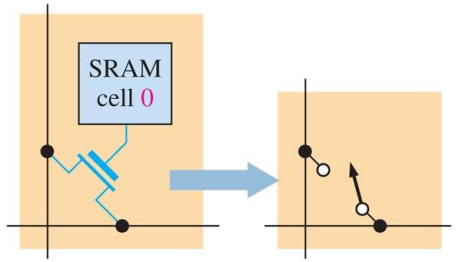
FIGURE 3-54 Concept of an AND array with SRAM technology.



(a) SRAM-based programmable array



(b) Transistor *on*



(c) Transistor *off*

FIGURE 3-55 Programming setup for reprogrammable logic devices.
(Photo courtesy of Digilent, Inc.)

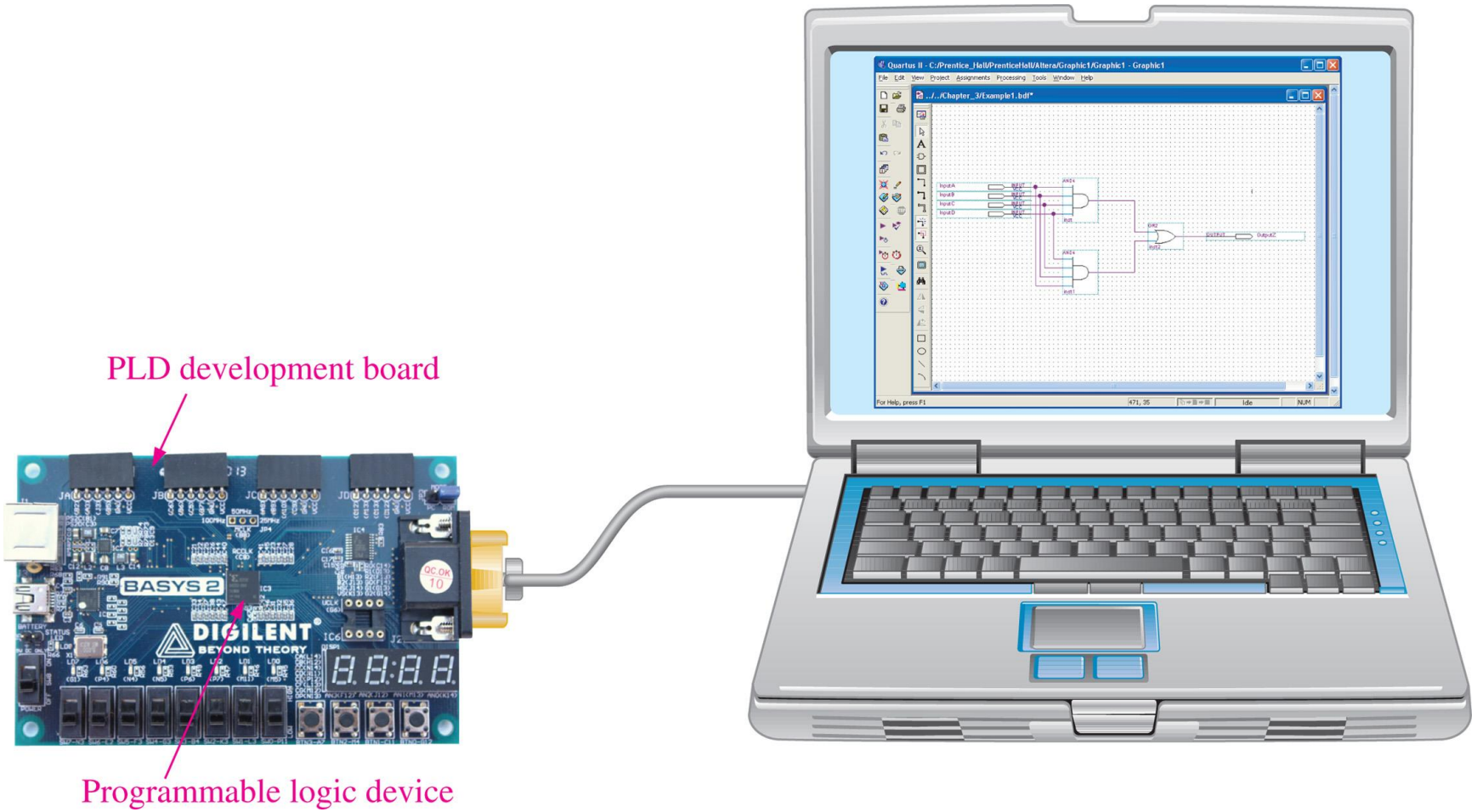


FIGURE 3-57 Simplified illustration of in-system programming via a JTAG interface.

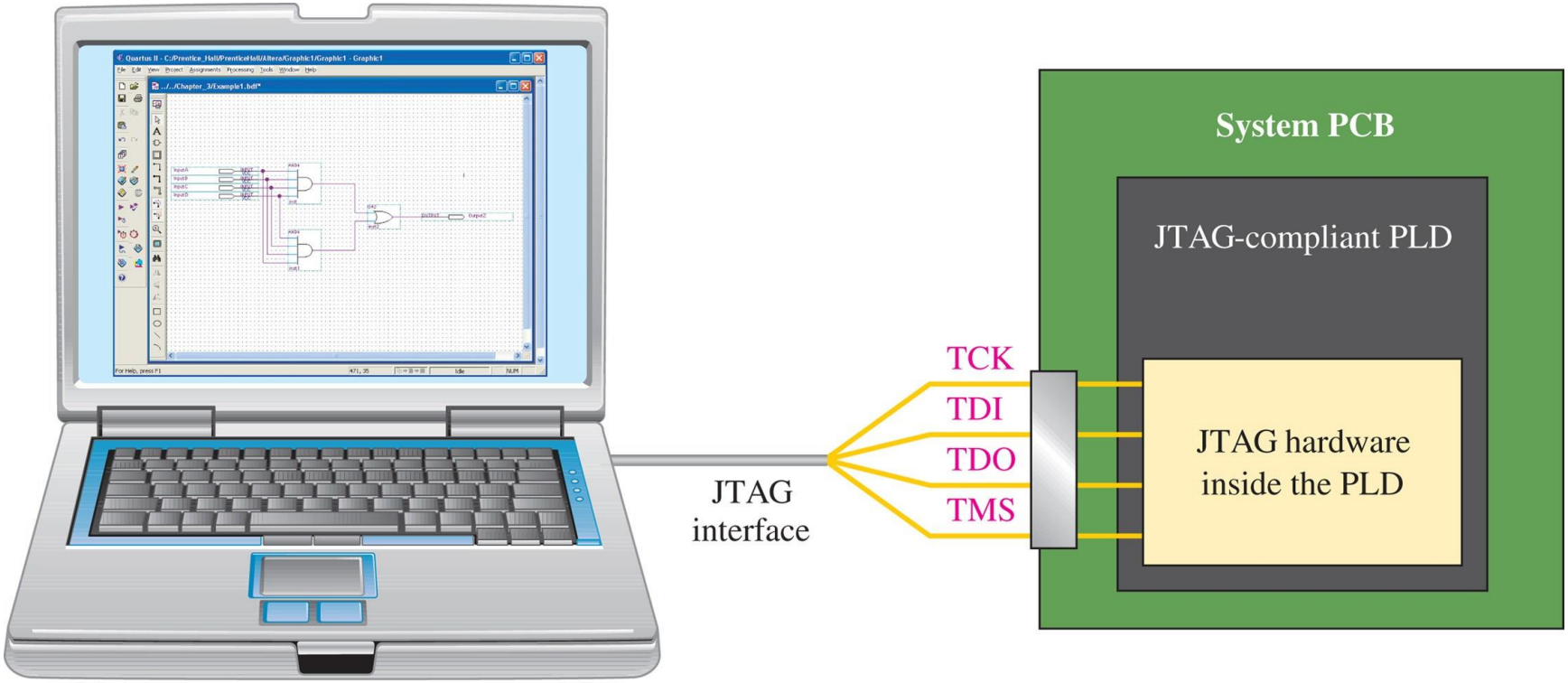
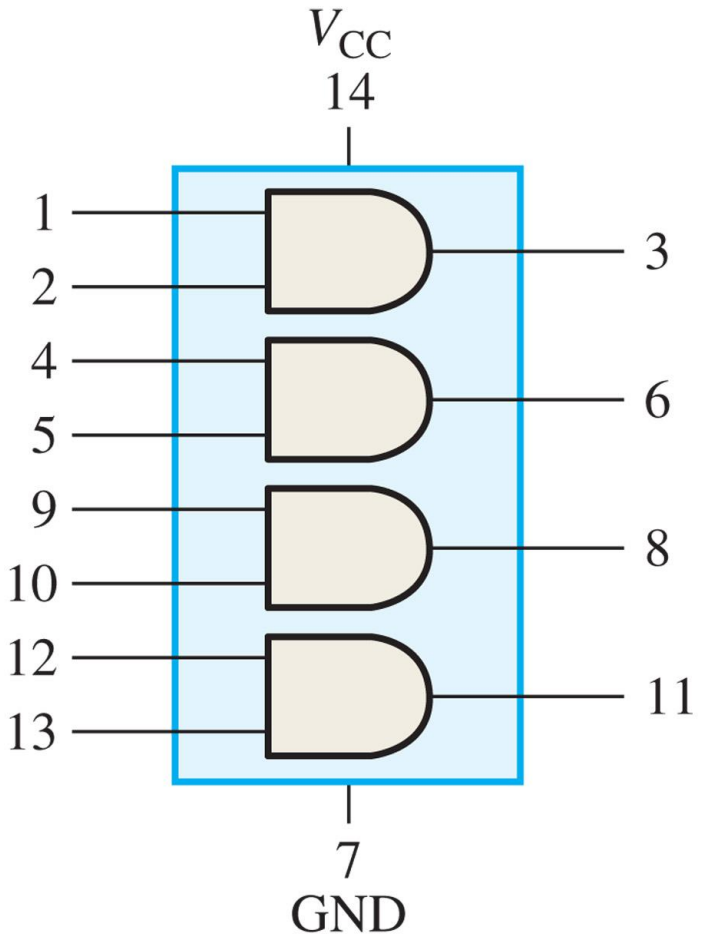
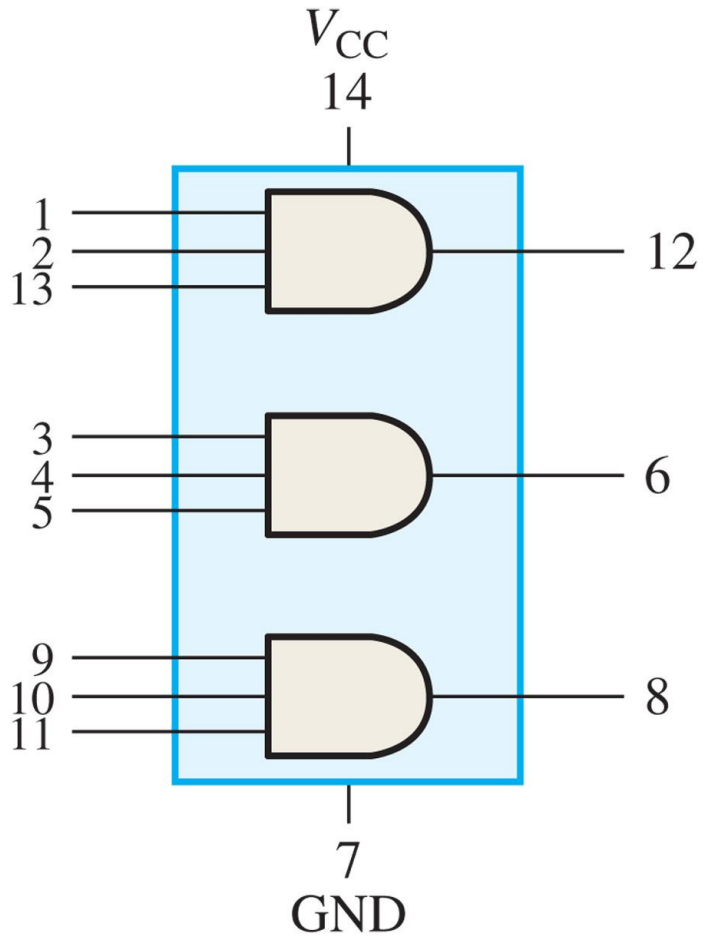


FIGURE 3-59 74 series AND gate devices with pin numbers.



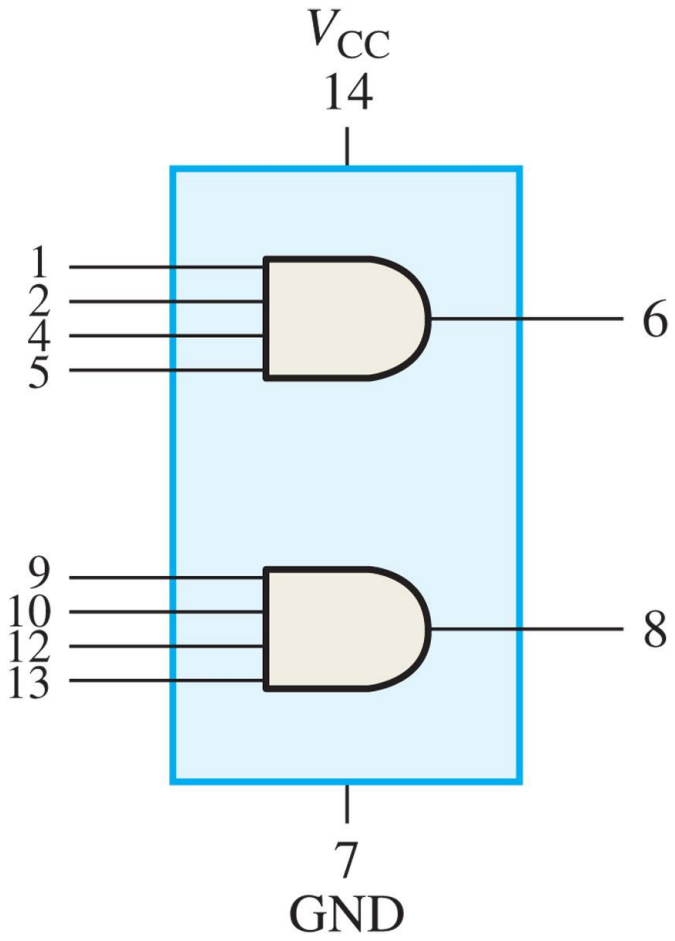
(a) 74xx08

FIGURE 3-59 (continued) 74 series AND gate devices with pin numbers.



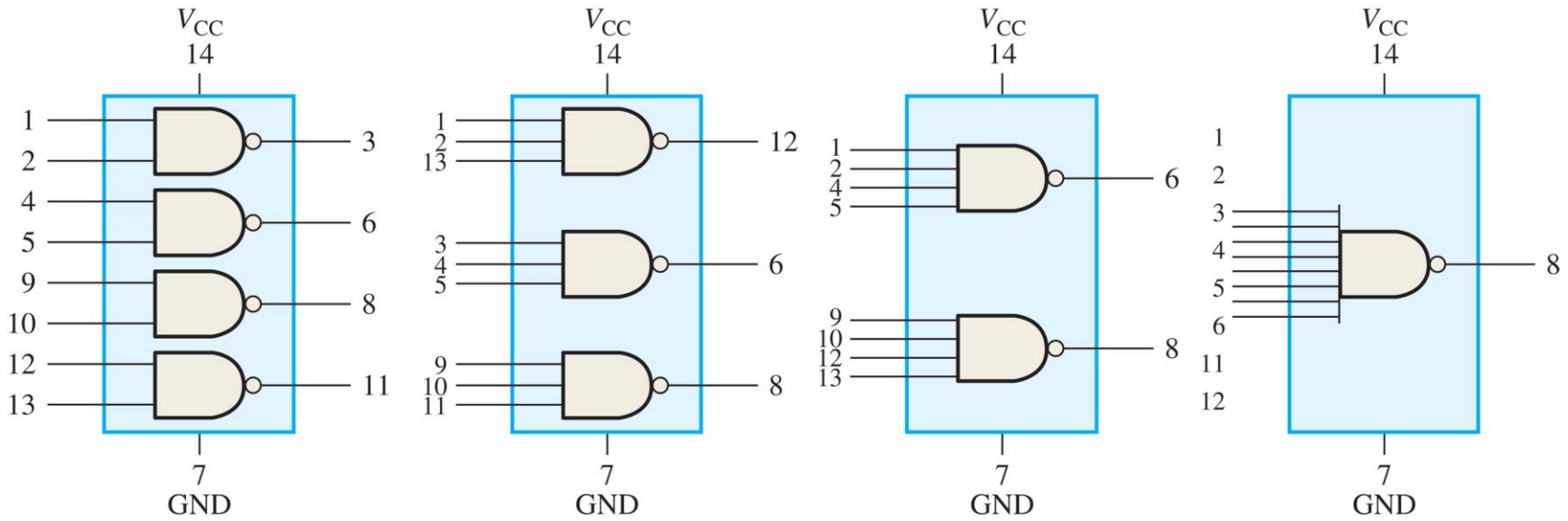
(b) 74xx11

FIGURE 3-59 (continued) 74 series AND gate devices with pin numbers.



(c) 74xx21

FIGURE 3-60 74 series NAND gate devices with package pin numbers.



(a) 74xx00 (b) 74xx10 (c) 74xx20 (d) 74xx30

FIGURE 3-61 74 series OR gate device.

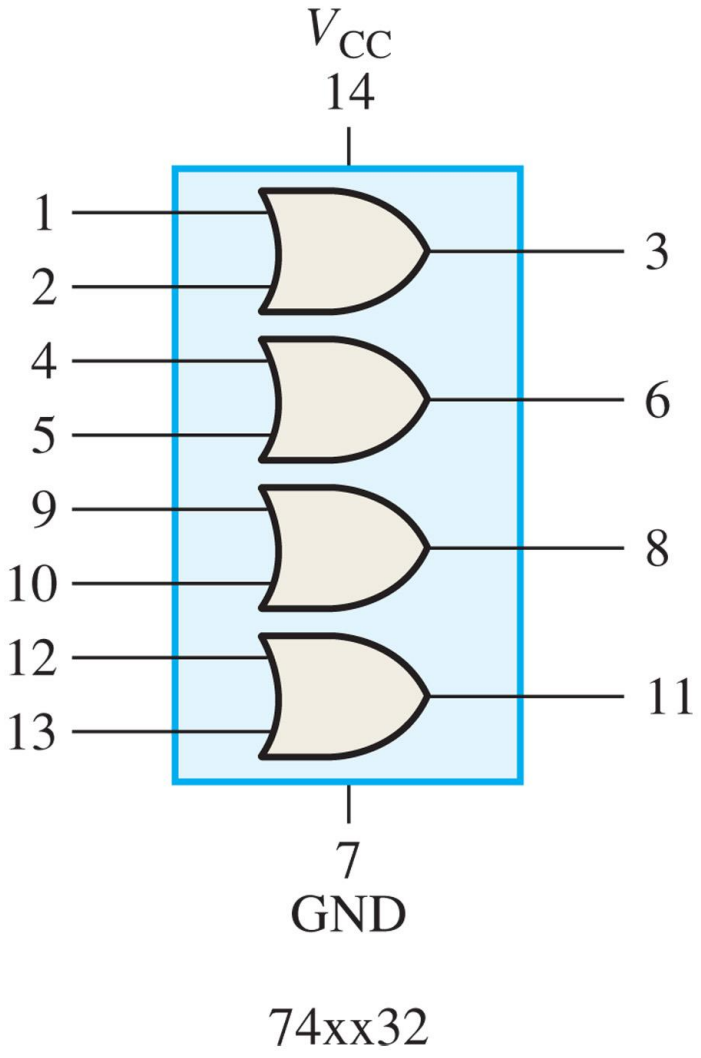


FIGURE 3-62 74 series NOR gate devices.

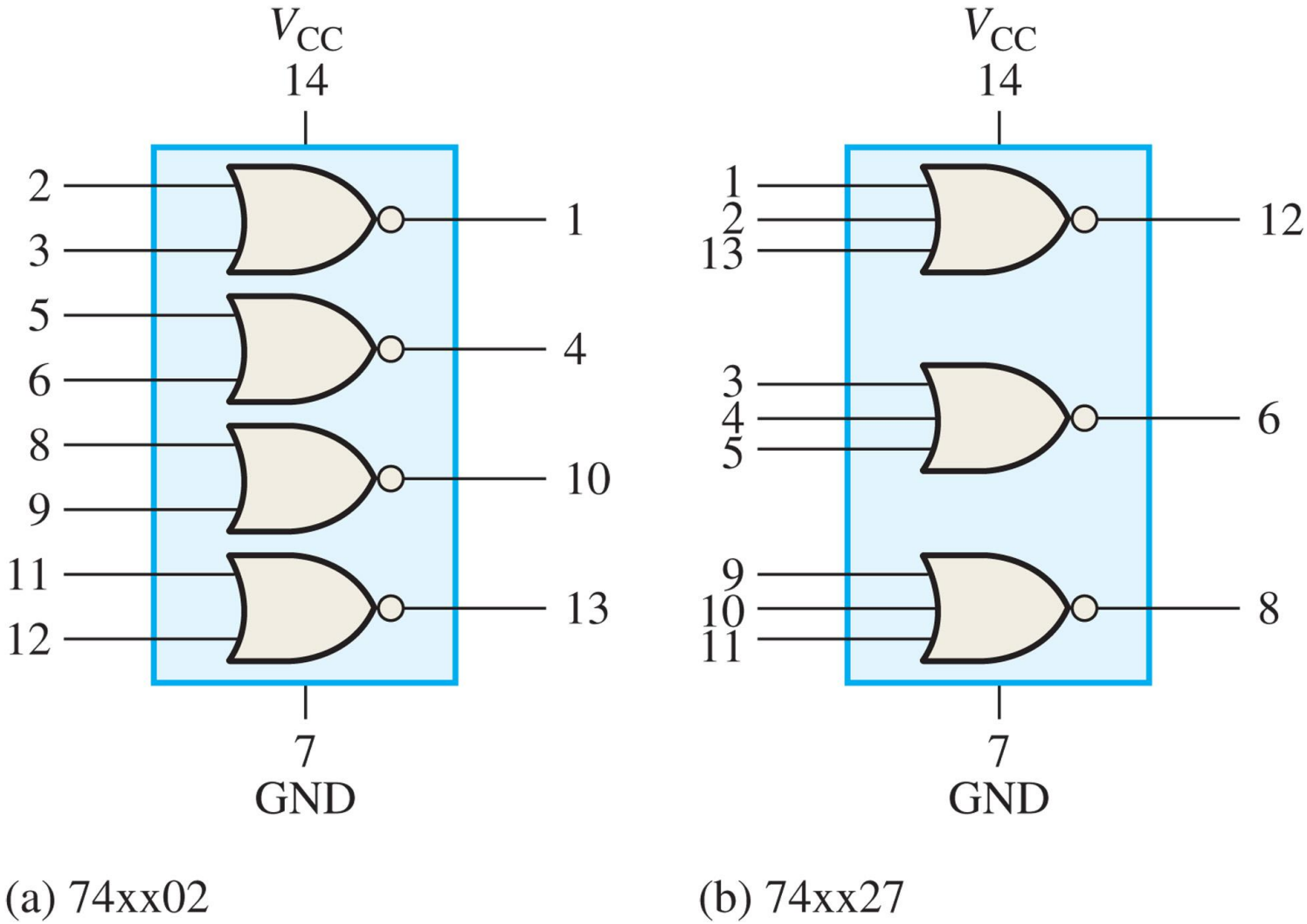


FIGURE 3-63 74 series XOR gate.

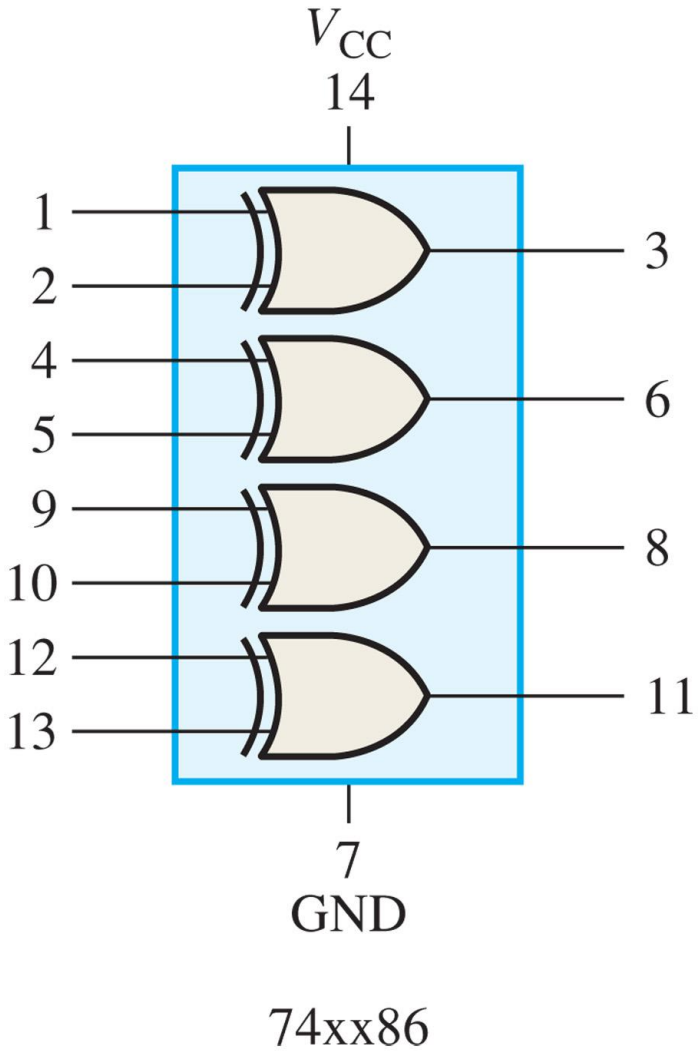
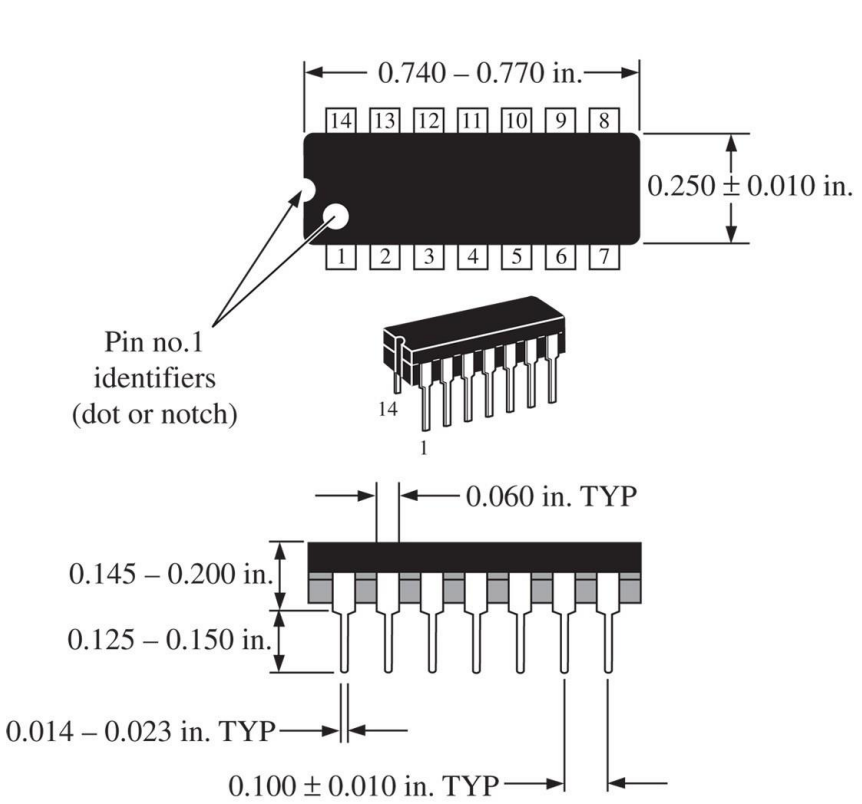
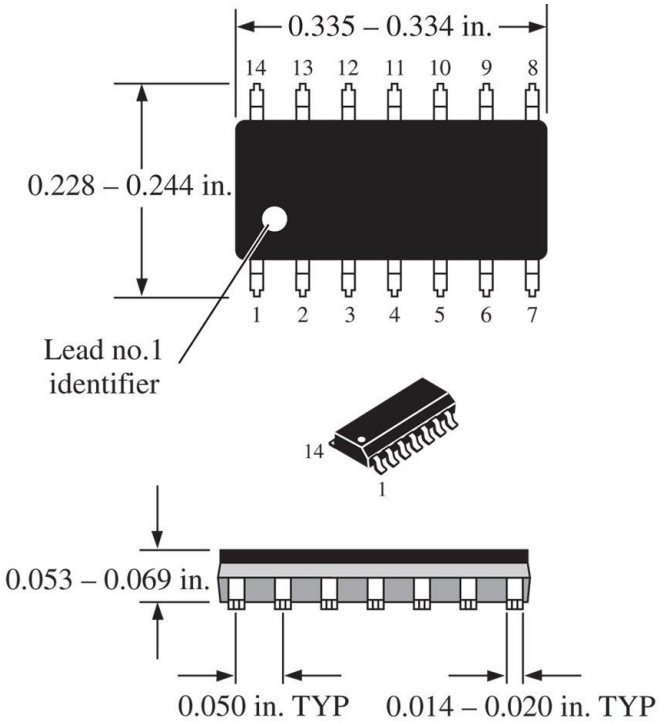


FIGURE 3-64 Typical dual in-line (DIP) and small-outline (SOIC) packages showing pin numbers and basic dimensions.



(a) 14-pin dual in-line package (DIP) for feedthrough mounting



(b) 14-pin small outline package (SOIC) for surface mounting

TABLE 3–14

74 series logic families based on circuit technology.

Circuit Type	Description	Circuit Technology
ABT	Advanced BiCMOS	BiCMOS
AC	Advanced CMOS	CMOS
ACT	Bipolar compatible AC	CMOS
AHC	Advanced high-speed CMOS	CMOS
AHCT	Bipolar compatible AHC	CMOS
ALB	Advanced low-voltage BiCMOS	BiCMOS
ALS	Advanced low-power Schottky	Bipolar
ALVC	Advanced low-voltage CMOS	CMOS
AUC	Advanced ultra-low-voltage CMOS	CMOS
AUP	Advanced ultra-low-power CMOS	CMOS
AS	Advanced Schottky	Bipolar
AVC	Advanced very-low-power CMOS	CMOS
BCT	Standard BiCMOS	BiCMOS
F	Fast	Bipolar
FCT	Fast CMOS technology	CMOS
HC	High-speed CMOS	CMOS
HCT	Bipolar compatible HC	CMOS
LS	Low-power Schottky	Bipolar
LV-A	Low-voltage CMOS	CMOS
LV-AT	Bipolar compatible LV-A	CMOS
LVC	Low-voltage CMOS	CMOS
LVT	Low-voltage biCMOS	BiCMOS
S	Schottky	Bipolar

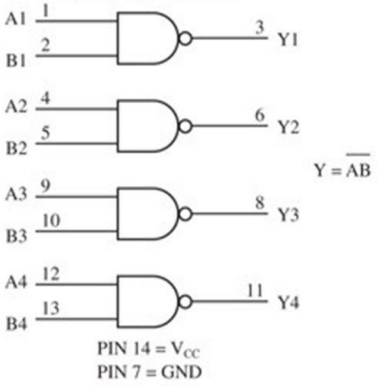
FIGURE 3-65 CMOS logic. Partial data sheet for a 54/74HC00A quad 2-input NAND gate. The 54 prefix indicates military grade and the 74 prefix indicates commercial grade.

Quad 2-Input NAND Gate High-Performance Silicon–Gate CMOS

The MC54/74HC00A is identical in pinout to the LS00. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 32 FETs or 8 Equivalent Gates

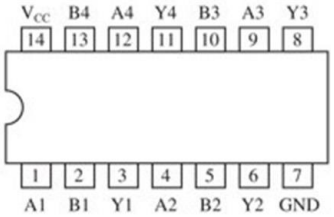
LOGIC DIAGRAM



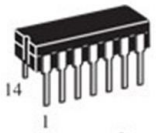
$Y = \overline{AB}$

PIN 14 = V_{CC}
PIN 7 = GND

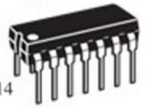
Pinout: 14–Load Packages (Top View)



MC54/74HC00A



J SUFFIX
CERAMIC PACKAGE
CASE 632-08



N SUFFIX
PLASTIC PACKAGE
CASE 646-06

D SUFFIX
SOIC PACKAGE
CASE 751A-03

DT SUFFIX
TSSOP PACKAGE
CASE 948G-01

ORDERING INFORMATION

MC54HCXXAJ	Ceramic
MC74HCXXAN	Plastic
MC74HCXXAD	SOIC
MC74HCXXADT	TSSOP

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
	TSSOP Package†	450	
T_{stg}	Storage Temperature	−65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	Plastic DIP, SOIC or TSSOP Package	260	
	Ceramic DIP	300	

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: – 10 mW/°C from 65° to 125° C
Ceramic DIP: – 10 mW/°C from 100° to 125° C
SOIC Package: – 7 mW/°C from 65° to 125° C
TSSOP Package: – 6.1 mW/°C from 65° to 125° C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		in	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

FIGURE 3-65 (continued) CMOS logic. Partial data sheet for a 54/74HC00A quad 2-input NAND gate. The 54 prefix indicates military grade and the 74 prefix indicates commercial grade.

DC CHARACTERISTICS (Voltages Referenced to GND) MC54/74HC00A

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit −55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1V or V_{CC} − 0.1V $\|I_{out}\| \le 20\mu A$	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1V or V_{CC} − 0.1V $\|I_{out}\| \le 20\mu A$	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 2.4mA$	3.0	2.48	2.34	2.20	
		$\|I_{out}\| \le 4.0mA$	4.5	3.98	3.84	3.70	
		$\|I_{out}\| \le 5.2mA$	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 2.4mA$	3.0	0.26	0.33	0.40	
		$\|I_{out}\| \le 4.0mA$	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 5.2mA$	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	6.0	1.0	10	40	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance		10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)	22	pF

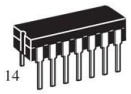
FIGURE 3-66 Bipolar logic. Partial data sheet for a 54/74LS00 quad 2-input NAND gate.

QUAD 2-INPUT NAND GATE

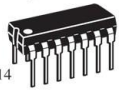
• ESD > 3500 Volts

SN54/74LS00

QUAD 2-INPUT NAND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08

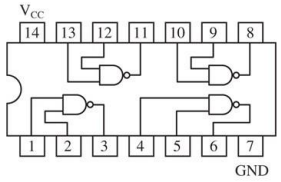


N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC



SN54/74LS00

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Ouput HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Ouput LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, I_N = 0.4 V
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				1.6	mA	V_{CC} = MAX
	Total, Output LOW				4.4		

NOTE 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		10	15	ns	

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

FIGURE 3-67

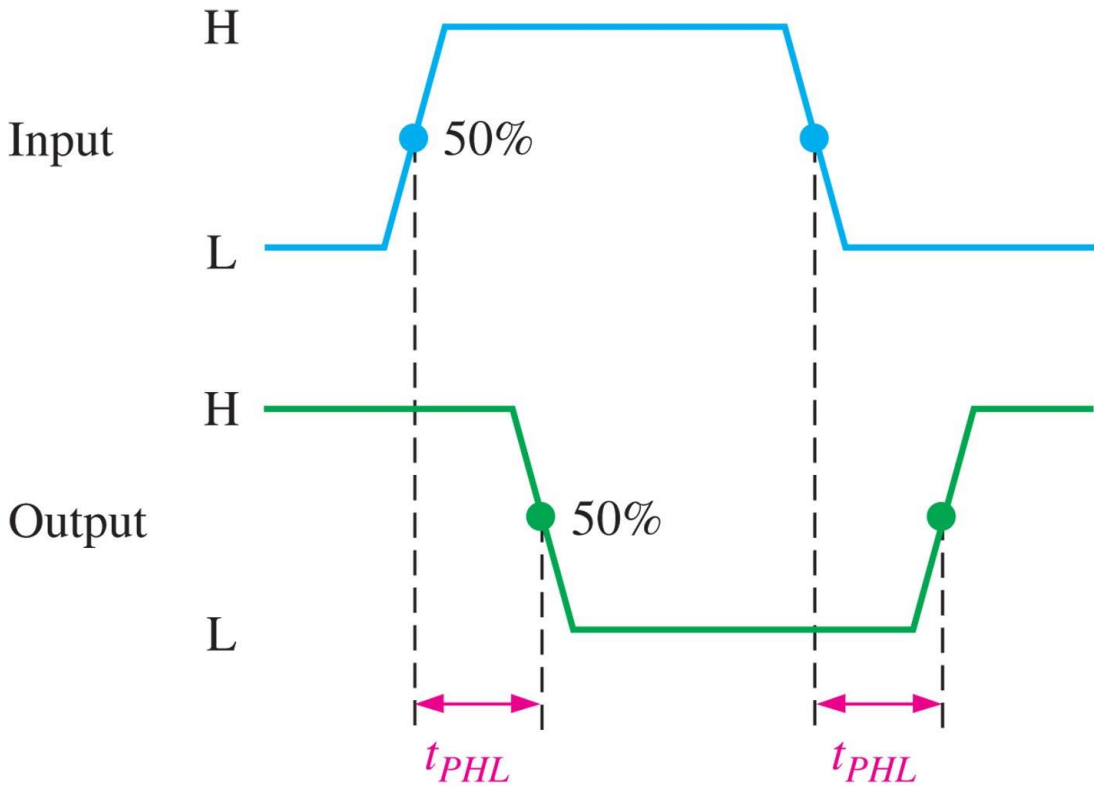


FIGURE 3-68 The LS family NAND gate output fans out to a maximum of 20 LS family gate inputs.

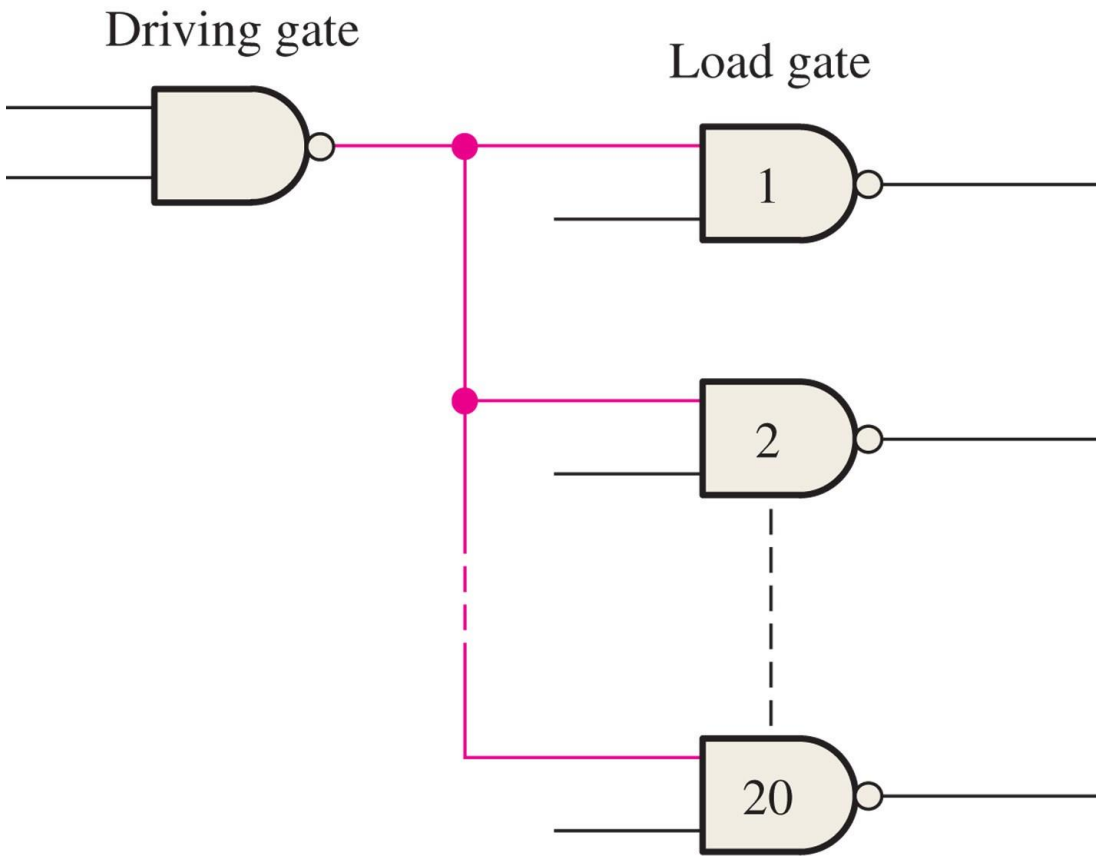
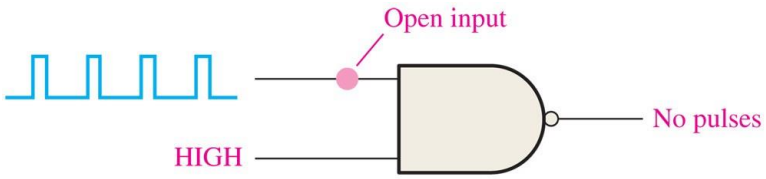
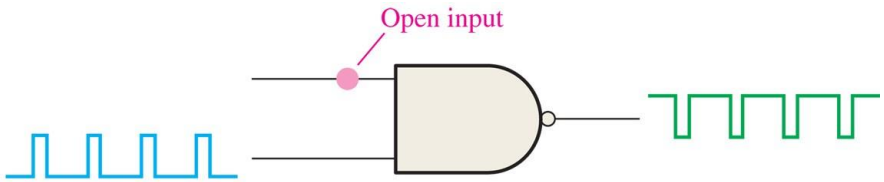


FIGURE 3-69 The effect of an open input on a NAND gate.

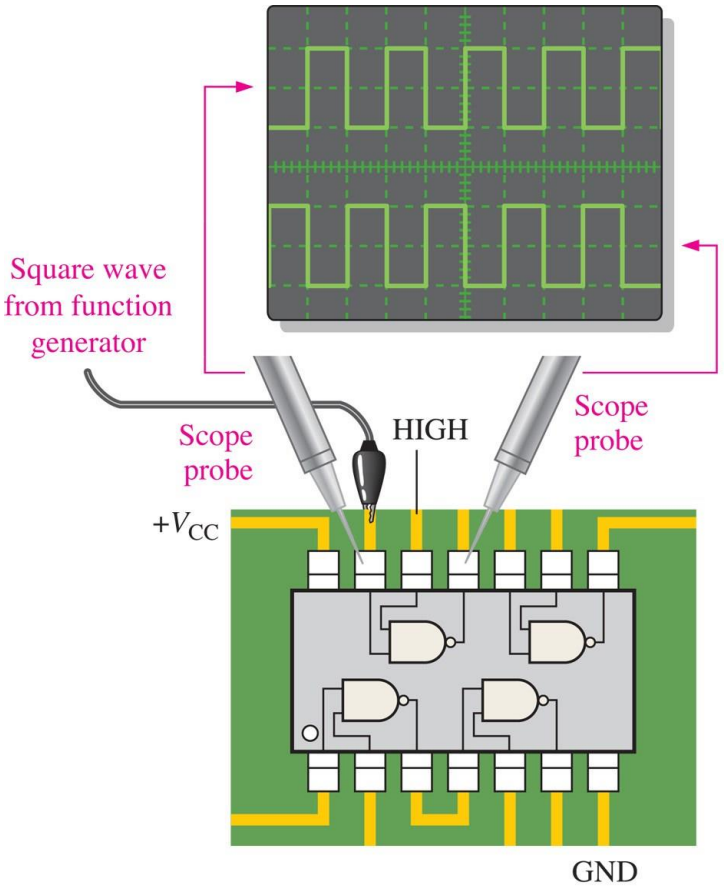


(a) Application of pulses to the open input will produce no pulses on the output.

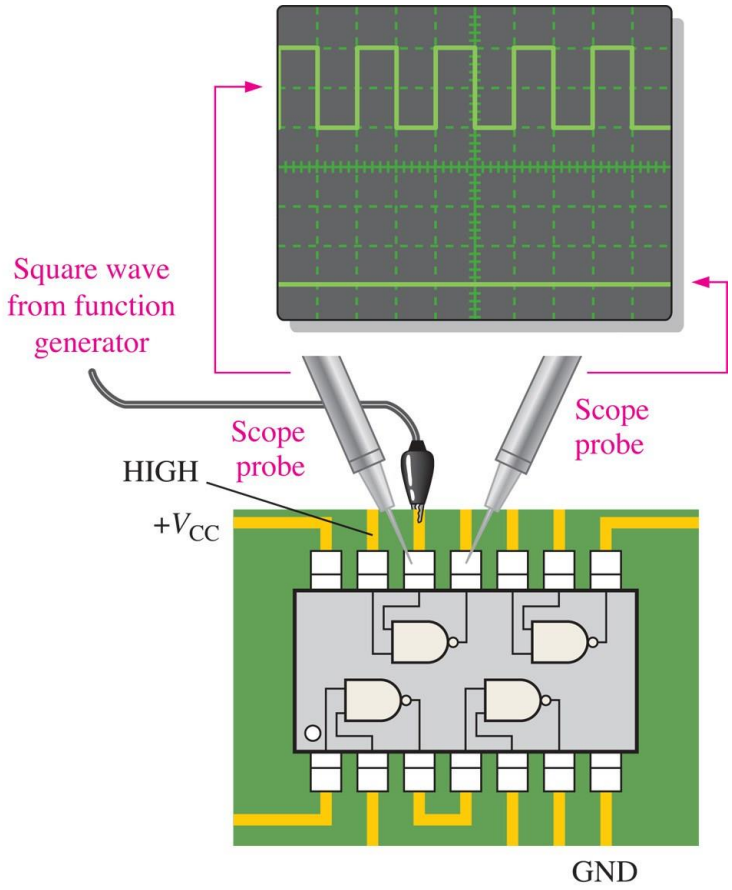


(b) Application of pulses to the good input will produce output pulses for bipolar NAND and AND gates because an open input typically acts as a HIGH. It is uncertain for CMOS.

FIGURE 3-70 Troubleshooting a NAND gate for an open input.

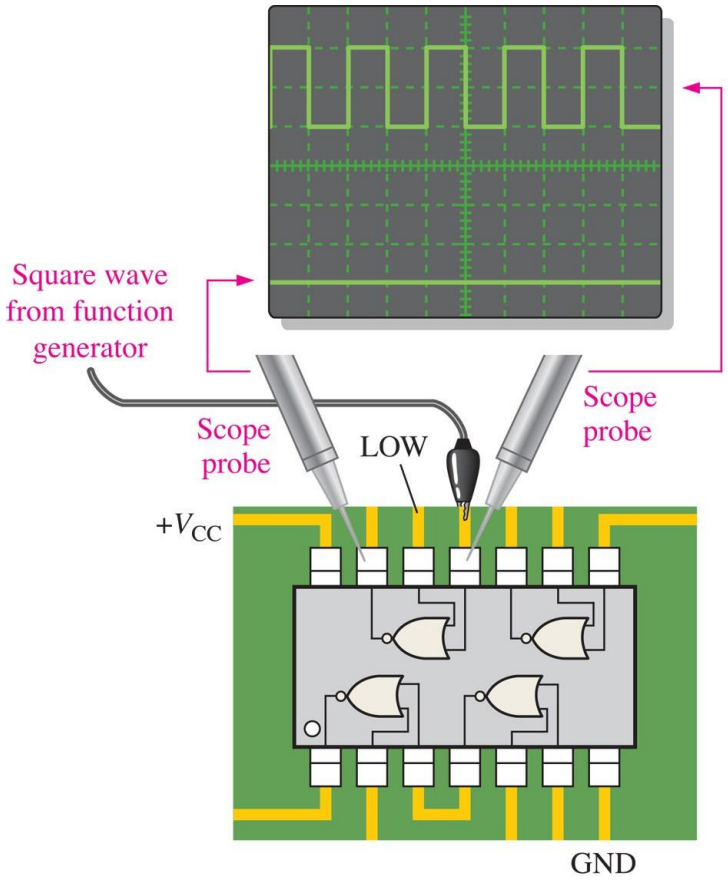


(a) Pin 13 input and pin 11 output OK

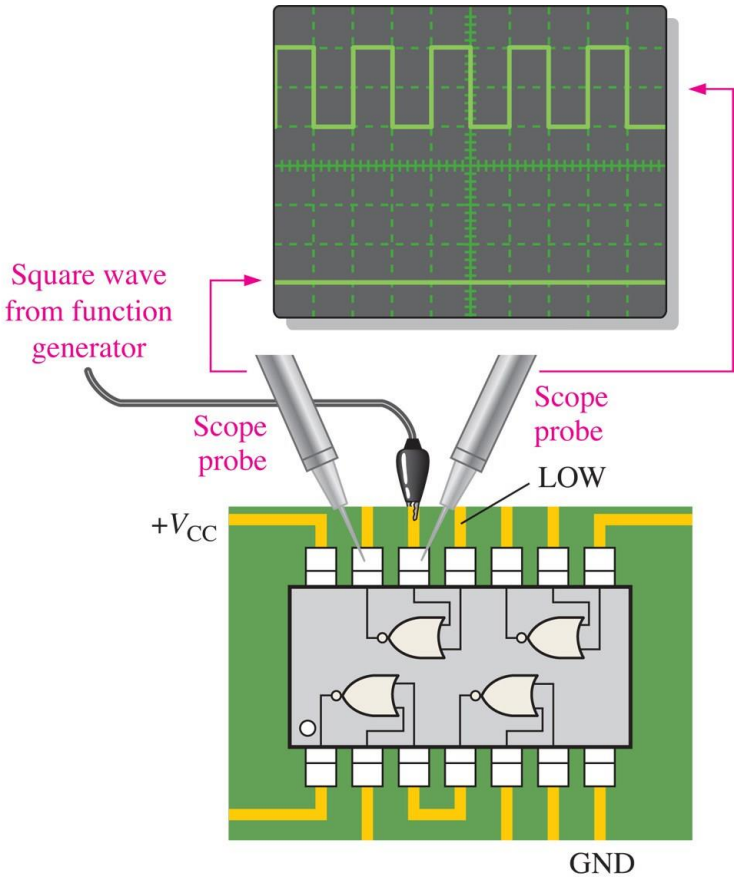


(b) Pin 12 input is open.

FIGURE 3-71 Troubleshooting a NOR gate for an open output.

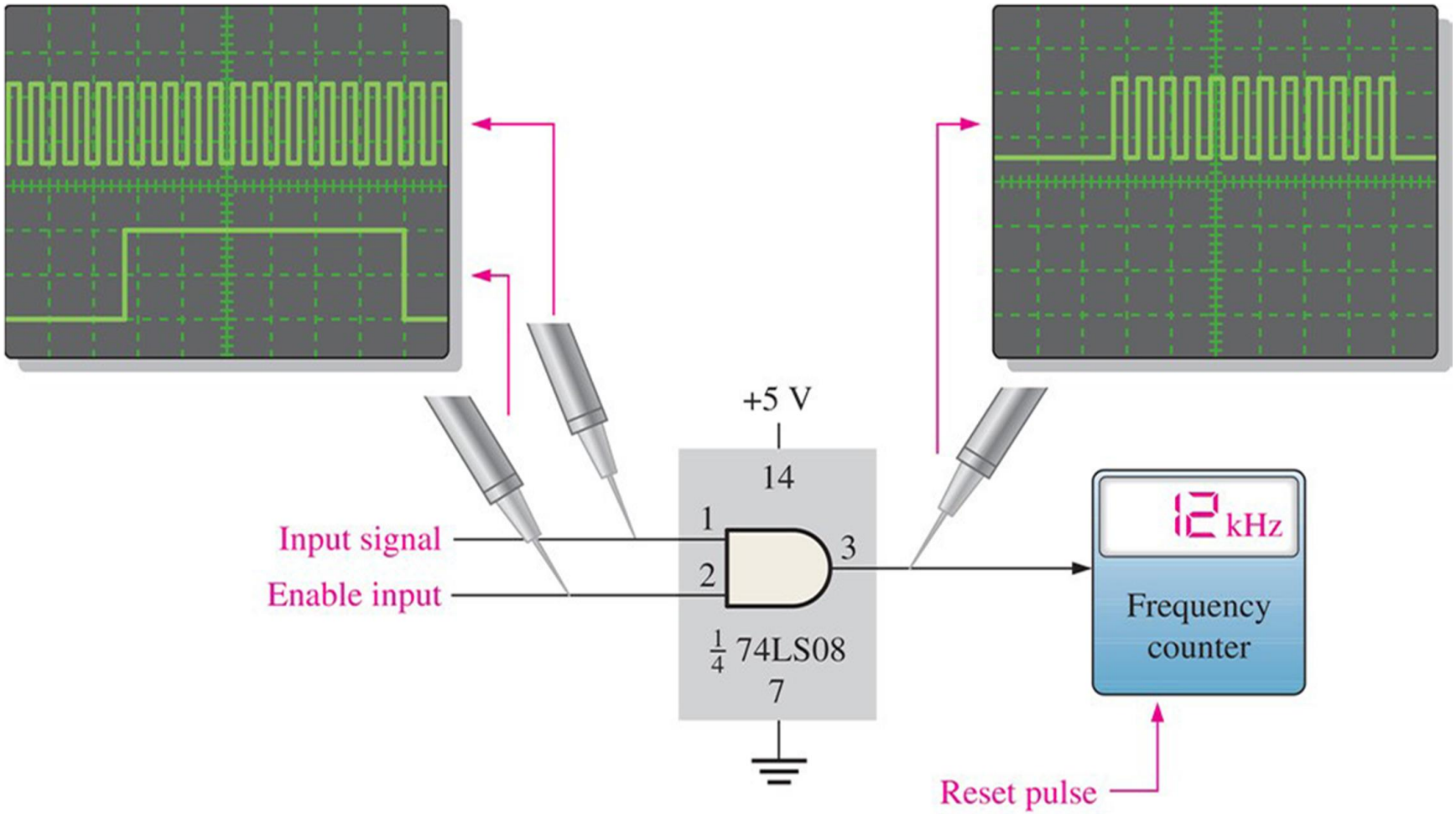


(a) Pulse input on pin 11. No pulse output.



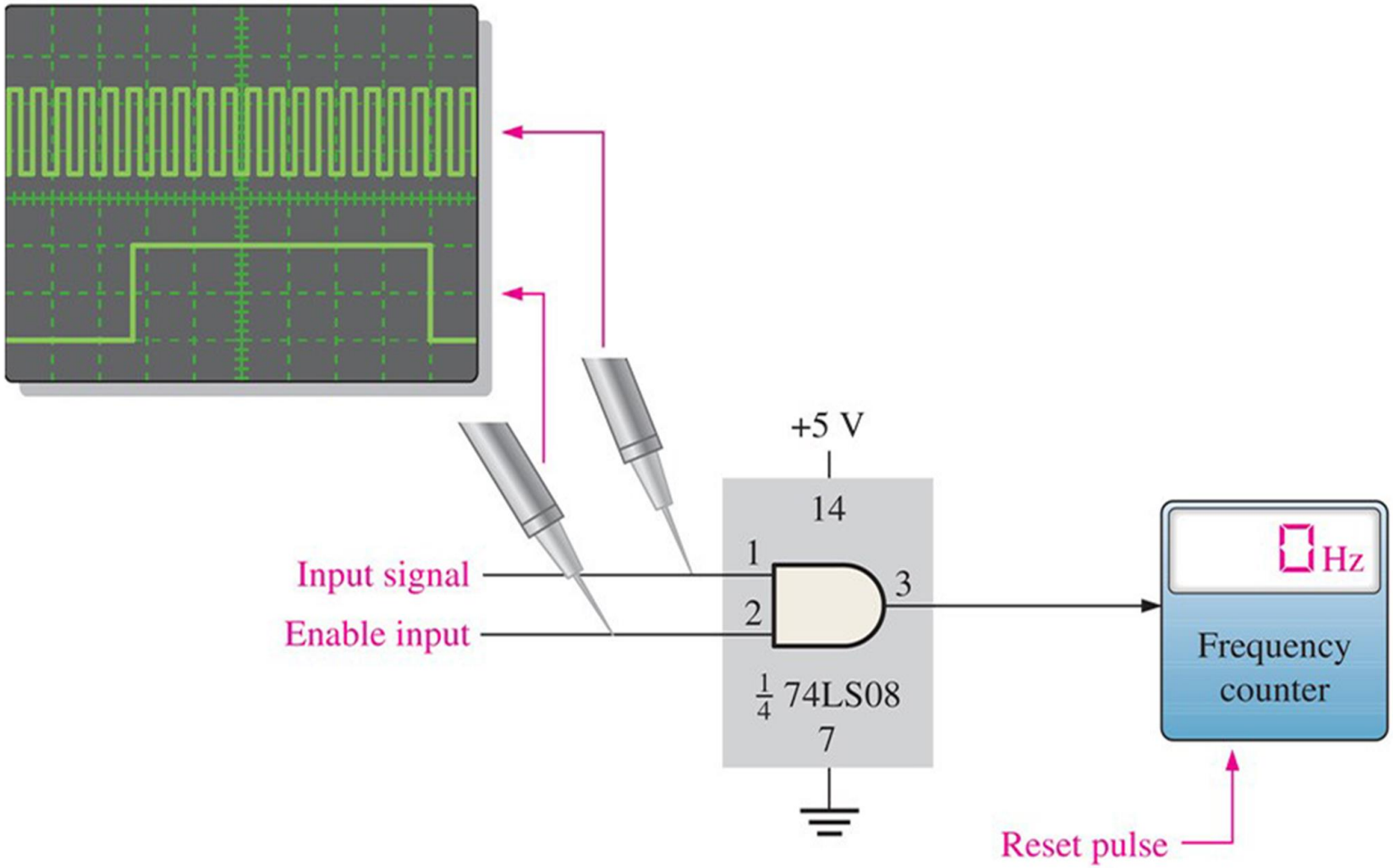
(b) Pulse input on pin 12. No pulse output.

FIGURE 3-73



(a) The counter is working properly.

FIGURE 3-73 (continued)



(b) The counter is not measuring a frequency.