Digital Fundamentals

Flip-flops and related devices
Objectives

- Use logic gates to construct basic latches
- Explain the difference between an S-R latch and a D latch
- Recognize the difference between a latch and a flip-flop
- Explain how S-R, D, and J-K flip-flops differ
- Explain how edge-triggered and master-slave flip-flops differ
- Understand the significance of propagation delays, set-up time, hold time, maximum operating frequency, minimum clock pulse widths, and power dissipation in the application of flip-flops
- Apply flip-flops in basic applications
- Analyze circuits for race conditions and the occurrence of glitches
- Explain how retriggerable and nonretriggerable one-shots differ
- Connect a 555 timer to operate as either an astable multivibrator or a one-shot
- Approach the debugging of a new design
- Troubleshoot basic flip-flop and one-shot circuits
- Describe the OLMCs in the GAL22V10 and the GAL16V8
- Explain the difference between the registered mode and the combinational mode
- Apply one-shots in a system application
bistable or multivibrator

**Figure 8--1** Two versions of SET-RESET (S-R) latches. Open file F08-01 and verify the operation of both latches.
Figure 8-2  Negative-OR equivalent of the NAND gate S-R latch in Figure 8-1(b).
Figure 8--3  The three modes of basic S-R latch operation (SET, RESET, no-change) and the invalid condition.

(a) Two possibilities for the SET operation

(b) Two possibilities for the RESET operation

- Momentary LOW
- Latch starts out RESET ($Q = 0$).
- No transitions occur because latch is already SET.

- Latch starts out SET ($Q = 1$).
- Outputs make transitions when $\bar{S}$ goes LOW and remain in same state after $\bar{S}$ goes back HIGH.

- Latch starts out SET ($Q = 1$).
- Outputs make transitions when $\bar{R}$ goes LOW and remain in same state after $\bar{R}$ goes back HIGH.

- Latch starts out RESET ($Q = 0$).
- No transitions occur because latch is already RESET.

- Simultaneous LOWs on both inputs
- HIGHs on both inputs

- Output states are uncertain when input LOWs go back HIGH.
Figure 8-4  Logic symbols for the S-R and S-R latch.

(a) Active-HIGH input S-R latch

(b) Active-LOW input S-R latch

\[ Q = \overline{S} + \overline{R} \]

<table>
<thead>
<tr>
<th>R</th>
<th>S</th>
<th>Q</th>
<th>( \overline{Q} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q</td>
<td>( \overline{Q} )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>SET</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Q</td>
<td>RESET</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

\[ \overline{Q} = Q + S \]
**Figure 8—5 Example:** Draw the waveform in the following situation

(a) Active-HIGH input S-R latch

(b) Active-LOW input S-R latch
Figure 8--6 The S-R latch used to eliminate switch contact bounce.
Figure 8--7  The 74LS279 quad S-R latch.
Figure 8--8  A gated S-R latch.

EN = enable

(a) Logic diagram  
(b) Logic symbol
Figure 8-9 Example: Determine the waveform!

(a) Logic diagram

(b) Logic symbol

S

EN

R

(a)

(b) Q

S

EN

R

Q
Figure 8--10  A gated D latch.

\[ D = \text{data} \]
Figure 8-11 Example: Determine the waveform!

(a) Logic diagram

(b) Logic symbol

(a) $D$

(b) $Q$

(a) $EN$

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Figure 8--12  The 74LS75 quad gated D latches.

(a) Logic symbol  (b) Truth table (each latch)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D$</td>
<td>$EN$</td>
<td>$Q$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$X$</td>
<td>0</td>
<td>$Q_0$</td>
</tr>
</tbody>
</table>

NOTE: $Q_0$ is the prior output level before the indicated input conditions were established.
Figure 8--13  **Edge-triggered** flip-flop logic symbols (top: positive edge-triggered; bottom: negative edge-triggered).

(a) S-R
(b) D
(c) J-K
Figure 8--14 Operation of a positive edge-triggered S-R flip-flop.

(a) $S = 1$, $R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $S = 0$, $R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

(c) $S = 0$, $R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)
Figure 8-15, 8-16 Example: Determine the waveforms
Figure 8--17  Edge triggering.

(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop

(b) A type of pulse transition detector
Figure 8--18  Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.

Triggering edge

CLK

S

HIGH (1)

1

0

Pulse transition detector

This gate is enabled.

This spike SETS flip-flop.

G₁

0

1

G₃

Q

1

0

G₂

HIGH

0

1

G₄

\bar{Q}

1

0

This gate is disabled because R is LOW.
Figure 8--19  Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.
Figure 8--20  A positive edge-triggered D flip-flop formed with an S-R flip-flop and an inverter.

<table>
<thead>
<tr>
<th>PRE</th>
<th>CLR</th>
<th>CLK</th>
<th>D</th>
<th>Q</th>
<th>Q̅</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>L</td>
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<tr>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>H↑</td>
<td>H↑</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>↑</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>↑</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>Q₀</td>
<td>Q₀̅</td>
</tr>
</tbody>
</table>

† This configuration is unstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.
Figure 8-21 Example: Determine the waveform!
Figure 8–22  A simplified logic diagram for a positive edge-triggered J-K flip-flop.
Figure 8-23  Transitions illustrating the toggle operation when $J = 1$ and $K = 1$. 
Figure 8-24 Example: determine the Q output!

### Function Table

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
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</thead>
<tbody>
<tr>
<td>PRE</td>
<td>CLR</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
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<tr>
<td>L</td>
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<tr>
<td>H</td>
<td>H</td>
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<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

*↑ The output levels are not guaranteed to meet the minimum levels for \( V_{OH} \). Furthermore, this configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.*

(a) CLK  
1 1 0 2 3 4 5

(b) J  
1 1 0 1 1 1

K  
0 1 0 1 0

Q  
1 0 0 1 0

Toggle  No change  Reset  Set  Set
Figure 8-25 Example: Determine the Q!

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRE</td>
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</tr>
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<td>H</td>
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<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
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<td>H</td>
<td>H</td>
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<td>H</td>
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<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

† The output levels are not guaranteed to meet the minimum levels for $V_{OH}$. Furthermore, this configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.
Figure 8--26  Logic symbol for a J-K flip-flop with active-LOW preset and clear inputs.
Figure 8--27  Logic diagram for a basic J-K flip-flop with active-LOW preset and clear inputs.
Figure 8-28 Example: Determine the Q waveform
Open file F08-28 to verify the operation.
Figure 8--29   Logic symbols for the 74AHC74 dual positive edge-triggered D flip-flops.

(a) Individual logic symbols

(b) Single block logic symbol
Note: The S and R inside the block indicate that PRE sets and CLR resets.
Figure 8--30  Logic symbols for the 74HC112 dual negative edge-triggered J-K flip-flops.
**Figure 8-31** Example: determine the 1Q waveform

**FUNCTION TABLE**

<table>
<thead>
<tr>
<th>PRE</th>
<th>CLR</th>
<th>CLK</th>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>Q̅</th>
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</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>L</td>
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<tr>
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<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
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<tr>
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<td>X</td>
<td>X</td>
<td>X</td>
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<td>H†</td>
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<tr>
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<td>↓</td>
<td>L</td>
<td>L</td>
<td>Q₀</td>
<td>Q₀</td>
</tr>
<tr>
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<td>H</td>
<td>↓</td>
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<td>L</td>
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<tr>
<td>H</td>
<td>H</td>
<td>↓</td>
<td>H</td>
<td>H</td>
<td>Toggle</td>
<td></td>
</tr>
<tr>
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<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Q₀</td>
<td>Q₀</td>
</tr>
</tbody>
</table>

†This configuration is unstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.

### Diagrams

(a) Individual logic symbols

(b) Single block logic symbol

---

**Waveforms**

(a) Pin 15 (1CLR)

(b) Pin 5 (1Q)

---

Pin 1 (1CLK)

Pin 2 (1J)

Pin 3 (1K)

Pin 4 (1PRE)
Figure 8--32  Basic logic diagram for a master-slave J-K flip-flop.
Figure 8--33  Pulse-triggered (master-slave) J-K flip-flop logic symbols.

(a) Active-HIGH clock: Data are clocked in on positive-going edge of clock pulse and transferred to output on the following negative-going edge.

(b) Active-LOW clock: Data are clocked in on negative-going edge of clock pulse and transferred to output on the following positive-going edge.
Figure 8-34 Example: determine the Q

(a) 

(b) 

SET  NC  RESET  NC  Toggle
Operating characteristics

Figure 8–35  Propagation delays, clock to output.
Figure 8--36  Propagation delays, preset input to output and clear input to output.
Figure 8--37  Set-up time \((t_s)\). The logic level must be present on the \(D\) input for a time equal to or greater than \(t_s\) before the triggering edge of the clock pulse for reliable data entry.
**Figure 8--38** Hold time ($t_{h}$). The logic level must remain on the $D$ input for a time equal to or greater than $t_{h}$ after the triggering edge of the clock pulse for reliable data entry.
Hands on tip (page 417)

CMOS can operate over wide power supply range typ. 2V to 6V. Therefore less expensive supplies can be used (compared to TTL). Smaller supply voltage means less power dissipation. Downside is the performance dependency on the supply voltage!
Figure 8-39  Example of flip-flops used in a basic register for parallel data storage.
Figure 8–40  The J-K flip-flop as a divide-by-2 device. $Q$ is one-half the frequency of CLK.

How do you create the same action with a D–flip-flop?
Figure 8--41  Example of two J-K flip-flops used to divide the clock frequency by 4. \( Q_A \) is one-half and \( Q_B \) is one-fourth the frequency of CLK.
Figure 8-42 Example 8-11: Develop the output waveform $f_{\text{out}}$
Figure 8--44  Flip-flops used to generate a binary count sequence. Two repetitions (00, 01, 10, 11) are shown.
Figure 8-45 Example 8-12: Determine the output waveforms

The diagram shows a JK flip-flop circuit with input and output waveforms. The clock input (CLK) is applied to the flip-flops, and the output waveforms for $Q_A$, $Q_B$, and $Q_C$ are depicted below the circuit.
A simple one-shot circuit.

Check out the simulation
**Figure 8--48** Basic one-shot logic symbols. $CX$ and $RX$ stand for external components.

X stands for external components
Figure 8--49  Nonretriggerable one-shot action.

(a) These pulses are ignored by the one-shot.
Figure 8--50  Retriggerable one-shot action.
Figure 8-51  Logic symbols for the 74121 nonretriggerable one-shot.

$R_{int} = 2 \text{ k}\Omega \text{ NOM}$

\[\text{logic symbol}^\dagger\]

\[\text{logic symbol}^\ddagger\]

$^\ddagger$This symbol is in accordance with ANSI/IEEE Std 31-1984 and IEC Publication 617-12.
Figure 8--52  Three ways to set the pulse width of a 74121.

(a) No external components
$R_{INT}$ to $V_{CC}$
$t_w = 30 \text{ ns}$

(b) $R_{INT}$ and $C_{EXT}$
$t_w = 0.7(2 \text{ k}$Ω$)C_{EXT}$

(c) $R_{EXT}$ and $C_{EXT}$
$t_w = 0.7R_{EXT}C_{EXT}$
Figure 8–53  Logic symbol for the 74LS122 retriggerable one-shot.

(a) Traditional logic symbol

(b) ANSI/IEEE std. 91–1984 logic symbol

(\(\times\) = nonlogic connection). \(\mathcal{N}\) is the qualifying symbol for a retriggerable one-shot.

The output pulse duration is primarily a function of the external capacitor and resistor. For \(C_{\text{ext}} > 1000\ \text{pF}\), the output pulse duration \(t_w\) is defined as:

\[
t_w = K \cdot R_T \cdot C_{\text{ext}} \left( 1 + \frac{0.7}{R_T} \right)
\]

where

- \(K\) is 0.32 for ‘122, 0.28 for ‘123 and ‘130

- \(R_T\) is in k\(\Omega\) (internal or external timing resistance.)

- \(C_{\text{ext}}\) is in pF

- \(t_w\) is in ns
Figure 8-54 Example: Create a oneshot with a pulse duration of 100 ms.

\[ t_W = 0.7 R_{EXT} C_{EXT} \]

\[ C_{EXT} = \frac{t_W}{0.7 R_{EXT}} = \frac{10^8 \text{ ns}}{0.7 \cdot 39 \text{ k}\Omega} = 3.66 \cdot 10^{-6} \text{ pF} = 3.66 \mu\text{F} \]
Application example

Figure 8–55  A sequential timing circuit using three 74LS122 one-shots.
Application example for a oneshot

**Active fuse**

instantaneous current spike (over current) initiates a pulse which is used to inhibit the current in some vital part of the circuit. The power is restored after the pulse goes low.
Figure 8--56  Internal functional diagram of a 555 timer (pin numbers are in parenthesis).
Figure 8--57  The 555 timer connected as a **one-shot**.

\[ t_w = 1.1R_1C_1 \]
Figure 8–58  One-shot operation of the 555 timer.

(a) Prior to triggering

(b) When triggered

(c) At end of charging interval
Figure 8--59  The 555 timer connected as an **astable multivibrator** (oscillator).
Figure 8--60  Operation of the 555 timer in the astable mode.
Figure 8-61  Frequency of oscillation as a function of $C_1$ and $R_1 1 2R_2$. The sloped lines are values of $R_1 1 2R_2$.

\[ f = \frac{1.44}{(R_1 + 2R_2)C_1} \]

\[ \text{Duty cycle} = \left( \frac{R_1 + R_2}{R_1 + 2R_2} \right) \times 100\% \]
Figure 8–62  The addition of diode $D_1$ allows the duty cycle of the output to be adjusted to less than 50 percent by making $R_1 < R_2$.

\[
\text{Duty cycle} = \left( \frac{R_1}{R_1 + R_2} \right) 100\%
\]
Figure 8-63 Example 8-16: Determine the frequency and the duty cycle (Open file F08-63 to verify operation).

Solution
5.64kHz
59.5%
Figure 8-64  Two-phase clock generator with ideal waveforms. Open file F08-64 and verify the operation.
Figure 8-65  Logic analyzer displays for the circuit in Figure 8-64.

(a) Logic analyzer display of CLK A and CLK B waveforms with glitches indicated by the “spikes”.

(b) Logic analyzer display showing propagation delay that creates glitch on CLK A waveform.
Figure 8–66  Two-phase clock generator using negative edge-triggered flip-flop to eliminate glitches. Open file F08-66 and verify the operation.
Hands on Tip

The glitches are usually very fast, short in duration signals and can be difficult to see on an oscilloscope. Logic analyzer are better suited for detecting glitches. Select latch mode or transitional sampling.
Figure 8-67  GAL block diagrams.
Figure 8--68  The GAL22V10 OLMC.
Figure 8--69  The GAL16V8 OLMC.

Emulation of most of the existing PALs
**Figure 8--70** Traffic light control system block diagram.
Figure 8--71  Block diagram of the timing circuits.
Figure 8-72

State decoder, output logic, and trigger logic from Chapter 6

Timing circuits
<table>
<thead>
<tr>
<th>Inputs $S_1$ $S_0$</th>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
<th>Case 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOW LOW</td>
<td>HIGH 25 s</td>
<td>LOW 10 kHz</td>
<td>HIGH 25 s</td>
<td>LOW 10 kHz</td>
</tr>
<tr>
<td>LOW HIGH</td>
<td>HIGH 4 s</td>
<td>HIGH 10 kHz</td>
<td>LOW 10 kHz</td>
<td>LOW 10 kHz</td>
</tr>
<tr>
<td>HIGH HIGH</td>
<td>HIGH 25 s</td>
<td>LOW 10 kHz</td>
<td>HIGH 25 s</td>
<td>LOW 10 kHz</td>
</tr>
<tr>
<td>HIGH LOW</td>
<td>HIGH 4 s</td>
<td>HIGH 10 kHz</td>
<td>LOW 10 kHz</td>
<td>LOW 10 kHz</td>
</tr>
</tbody>
</table>
SUMMARY

Figure 8--74

(a) Active-HIGH input S-R latch
(b) Active-LOW input S-R latch
(c) Gated S-R latch
(d) Gated D latch

(e) S-R edge-triggered flip-flops
(f) D edge-triggered flip-flops
(g) J-K edge-triggered flip-flops
(h) J-K master-slave flip-flops